DATA PRODUCTS DIVISI
MODEL 8520
PORTABLE TIME CODE
GENERATOR

SYSTRON DONNER

The design information contained herein is the sole property of Systron-Donner Corporation. The disclosure of this information does not constitute the release of proprietary rights thereof, but is to be used for information purposes only when necessary. Permission to reproduce this information or the product described herein must be obtained in writing from the SYSTRON-DONNER CORPORATION, 888 Galindo Street, Concord, California 94520

© 1969 Systron-Donner Corporation

PROPERTY OF DEPT. 8-270
METROLOGY LAB.
DO NOT REMOVE
FROM AREA
REC'D 1-13-71

DATA PRODUCTS DIVISION
MODEL 8520
PORTABLE TIME CODE
GENERATOR

ERRATA

MODEL 8520/8521/8585

Dwg. #41046-7-1 XR3 DC Code Generator is added to the Standard Model 8520 manual to cover Option C26A.

Power Supply Dwg. #31248-7-1 E replaces Dwg. #31248-7-1 D, 31214-7-2 A, 31151-7-1, 31183-7-2 A in the Standard Model 8520 manual.

Wiring Block Diagram Dwg. #21792-7-1 has been replaced by Dwg. #31892-7-1 B.

Dwg. #41061-7-1 is added to cover Option C26 and C26A and should be used in place of Dwg. #31892-7-1 B when either option is used.

CAUTION

MARK PAGES 6-9 thru 6-12, AND PAGE 6-52 WARNING DO NOT USE

Dwgs. #31033-7-1, 31154-7-1, 21219-4-1, 21219-7-1, 21223-4-1, 21223-7-1, 21228-4-1, 31033-4-1, 31154-4-1 has been added to cover the Model 8585 Remote Control/Display Unit which may be used with either the Model 8520 or 8521. Also added is "Interconnect Requirements - Model 8585" in Chapter 2 page 2-4.

Changes effected to the standard Model 8520 manual:

Delete	Title	Insert
Pages 6-9, 6-10, 6-11, 6-12,6-52		
	Interconnect Requirements- Model 8585	page 2-4
	Errata Drawings Title Page	1 of 14
	Dwg. #41046-7-1	2 of 14
	Dwg. #31248-7-1	3 of 14
	Dwg. #31892-7-1	4 of 14
	Dwg. #41061-7-1	5 of 14
	Dwg. #31033-7-1	6 of 14
	Dwg. #31154-7-1	7 of 14
	Dwg. #21219-4-1	8 of 14
	Dwg. #21219-7-1	9 of 14
	Dwg. #21223-4-1	10 of 14
	Dwg. #21223-7-1	11 of 14
	Dwg. #21228-4-1	12 of 14
	Dwg. #31033-4-1	13 of 14
	Dwg. #31154-4-1	14 of 14

TABLE OF CONTENTS

MODEL 8520

		PAGE
CHAPTER 1	GENERAL DESCRIPTION	
1.1	Basic Functions	1-1
1.2	Portable Features	1-1
1.3	Standard Features	1-2
1.4	Applications	1-5
1.5	Standard Optional Features	1-6
1.6	Required Feature Model 8521 Only	1-8
CHAPTER 2	INSTALLATION	
2.1	Initial Inspection	2-1
2.2	Storage and Reshipment	2-1
2.3	Installation	2-2
2.4	Power Requirements	2-2
CHAPTER 3	OPERATION	
3.1	General	3-2
3.2	Use of Controls, Indicators, and Connectors	3-2
3.2.1	Power Switch	3-2
3.2.2	Battery Display Switch	3-3
3.2.3	Mode Control	3-3
3.2.3.1	Preset S3 (Fast or Slow)	3-3
3.2.3.2	Reset S4	3-4
3.2.3.3	Start Run Min Hr Stop Switch S7	3-4
3.2.4	Clock Adjust	3-5
3.2.5	Time Display	3-6
3.2.6	Mod Code J3	3-6
3.2.7	DC Code J4	3-6
3.2.8	Pulse Rate Outputs J6, J7, J8	3-6
3.2.9	Ext Sync J5	3-6
3.3	Operation	3-7
3.3.1	Turn on Procedure	3-7
3.3.2	Reset Procedure	3-7
3.3.3	Preset Time Procedure	3-7
3.3.4	Stop Procedure	3-8
3.3.5	Manual Start Procedure	3-8
3.3.6	Automatic Start Procedure	3-9
3.3.7	Synchronization Procedure	3-10
CHAPTER 4	MAINTENANCE AND CALIBRATION	
4.1	Factory Service	4-1
4.2	Routine Maintenance	4-1
4.3	Printed-Circuit Board Repair	4-2
4.4	Logic Functions	4-3

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_06059

Table of Contents
(continued)

Chapter 4 (con't)

4.5	JK-Type Flip-Flop	4-6
4.6	Operational Test & Calibration Procedure	4-6
4.6.1	Recommended Test Equipment	4-7
4.6.2	Power Supply Dwg. #31248-7-1 and Dwg. #31214-7-2	4-7
4.6.3	Switching Regulator Dwg. #31248-7-1 and Dwg. #31214-7-2	4-8
4.6.4	AC Supply Dwg. #31151-7-1	4-8
4.6.5	Time Base and Oscillator Dwg. #31209-7-2	4-8
4.6.6	Adv/Ret Synchronizer Dwg. #31209-7-2	4-10
4.6.7	Control, Input/Output	4-10

CHAPTER 5 OVERALL FUNCTIONAL DESCRIPTION

5.1	Time Base Adv/Ret Synchronizer	5-1
5.2	Time Base, Minor Counters	5-1
5.3	Time-of-Day Accumulator	5-2
5.4	Code Generator	5-2
5.5	Dual Shaper Modulator	5-2

CHAPTER 6 CIRCUIT DESCRIPTION AND ILLUSTRATIONS

6.1	Power Supply Dwg.#31248-7-1, Dwg. #31214-7-2, #31151-7-1 C, Dwg. #31183-7-2	6-2
6.2	Time Base/Adv-Ret Synchronizer Dwg. #31209-7-2	6-13
6.3	Time Base/Minor Counter Dwg. #31210-7-1,2,3	6-20
6.4	Switchable IRIG DC Code Generator Dwg. #31044-7-5	6-25
6.5	Time-Of-Day Accumulator Dwg. #31501-7-2	6-33
6.6	Dual Shaper Modulator Dwg. #31216-7-4	6-39
6.7	Front Panel Readout Dwg. #31195-7-2	6-44

LIST OF TABLES

TABLES	*DESCRIPTION*	*PAGE*
1-1	Portable Features	1-2
1-2	Model 8520 Portable Time Code Generator	1-2
1-3	8500 Series Standard Options	1-6
4-1	Oscillator Accuracy	4-9

LIST OF FIGURES

FIGURE NO.	*DESCRIPTION*	
3.1	Time Code Generator Standard Model 8520	3-1
4.1	Oscillator Accuracy Test	4-9
4.2	Adv/Ret Synchronizer Test	4-10
4.3	WWV Sync Circuit Test	4-11
4.4	Tune Control Adjustment	4-12
6.1	Timing Sequence Time Base/Adv-Ret Synchronizer	6-15
6.2	Timing Diagram Switchable IRIG DC Code 31581-7-1	6-29
6.3	Timing Diagram Switchable IRIG DC Code 31581-7-1	6-30

LIST OF SCHEMATICS

Schematic No.	*Description*	
31248-7-1	Schematic, Power Supply	6-9
31214-7-2 A	Schematic, Switching Regulator	6-10
31151-7-1	Schematic, AC Power Supply	6-11
31183-7-2 A	Schematic, Heater Circuit	6-12
31209-7-2 D	Schematic, Time Base/Adv-Ret Synchronizer	6-19
31210-7-1 G	Schematic, Time Base/Minor Counters	6-24
31044-7-5 A	Schematic, IRIG B DC Code Generator	6-32
31501-7-2	Schematic, Time-of-Day Accumulator	6-38
31216-7-4 A	Schematic, Dual Shaper Modulator	6-43
31195-7-2 A	Schematic, Readout	6-46
21792-8-1	Models 8520 & 8521 System Block Diagram	6-47
	Optional Codes and Code Formats	6-48 thru 6-51
21792-7-1	Models 8520-8521 Wiring Block Diagram	6-52

MODEL 8520

CHAPTER 1

GENERAL DESCRIPTION

1.1 BASIC FUNCTIONS

The Model 8520 is an extremely rugged, integrated circuit logic (discrete components used where required) Portable Time Code Generator (PTCG) which generates the standard serial time code Inter Range Instrumentation Group "B" (IRIG B) or XR 3 (optional) Binary Coded Decimal (BCD) Format and displays them in terms of hours, minutes, and seconds and provides outputs to drive other displays.

IRIG B or XR-3 (optional) Time Codes are provided as both a modulated format and a dc level shift output. Pulse outputs of 1000 pps, 100 pps and 1 pps are available at BNC connectors on the unit front panel. Time-of-day information may also be provided as parallel BCD outputs for remote displays and/or remote controls and display units (option E15).

An External pulse input allows for synchronization to an external source such as WWV, and Advance/Retard circuitry allows for retaining synchronization after initial start coincidence.

1.2 PORTABLE FEATURES

Some portable features are cited in Table 1.1

TABLE 1-1

PORTABLE FEATURES

Self-contained Numeric Display (Hrs., Min., Sec.).

Light Weight:	15 pounds
Small Size:	4-7/8" wide 7-5/8" high 12-1/2" deep handles add approximately 1-1/2" to height.

All operating Controls for Start/Stop, Preset, Reset, Advance/Retard, Battery Display, etc. (Self-contained 45 minute rechargeable Battery Pack).

1.3 STANDARD FEATURES

The Model 8520 PTCG is designed for simple reliable operation, long life, and easy maintenance. Its circuitry is fully solid-state and constructed on printed circuit plug-in modules. It has a six-digit in-line readout which displays time-of-day information continuously in terms of hours, minutes, and seconds.

A brief summary of the Model 8520 PTCG standard features is cited in Table 1.2 and are elaborated on in other areas of this manual.

TABLE 1-2

MODEL 8520 PORTABLE TIME CODE GENERATOR

SERIAL TIME CODE:

IRIG "B" or XR-3 (optional) Format in terms of BCD hours, minutes, and seconds.

MODULATED CODE:

Carrier Frequency: IRIG "B" - 1 kHz; XR 3 1 kHz or 250 Hz.

Level - Adjustable from 0 to 10 volts peak-to-peak from a low impedance 15 mA current source.

TABLE 1-2
(continued)

Modulation Ratio: 3:1 nominal, adjustable from 2:1 to 6:1.

Connector - Front panel BNC.

DC LEVEL SHIFT:

0 ± 0.4 V dc to +5 volt dc peak from a 5 mA source.

Connector - Front panel BNC

DISPLAY:

Six (6) miniature in-line display tubes display time of day in terms of hours, minutes, and seconds.

TIME BASE:

1 MHz crystal controlled oscillator

STABILITY:

Aging rate 1 part 10^7 per day. 1 part 10^5 -20°C to +55°C with zero warm up time.

PULSE OUTPUTS:

1000 pps, 100 pps, 1 pps leading edge "on time".

LEVEL:

0 ± 4 V dc to a +5 V dc peak from a 5 mA source. Rise time 0.5 microseconds.

TABLE 1-2
(continued)

CONNECTOR:

Front Panel BNC

SYNCHRONIZATION:

From an external 1 pps such as WWV tick envelope.

Connector - Front panel BNC.

POWER:

12 to 50 V dc; 0.7 amp at 28 V dc. 117/230 V ac ±10% 50-400 Hz OPTIONAL.

Connector - Front panel PT02A-14-5 P (PT06A-14-5S (SR) mating connector) supplied.

PACKAGING:

4-7/8" wide x 7-5/8" high x 12-1/2" deep. Feet and handle and approximately 1-1/2" to height.

MANUAL CONTROLS:

Power - ON/OFF Switch, Locking toggle, Power Fuse, and Indicator.

Mode Control *START RUN MIN HR STOP Rotary Switch
*PRESET (HR or MIN) FAST 5/second, Slow 1/second momentary toggle switch
*RESET (HR MIN) Monentary toggle switch

Clock Adjust *ADVANCE/RETARE momentary switch
*PER SEC Rotary rate selector of 100 ms, 10 ms, 1 ms, 100 µs and OFF.

TABLE 1-2
(continued)

Battery Display - Momentary Toggle Switch

ENVIRONMENTAL:

Shock/Vibration - Mil E5400 Class II

Humidity - 95% (no condensation)

Operating Temperature - -20°C to +65°C

Storage Temperature - -55°C to +100°C

RFI:

Mil 6181D

1.4 APPLICATIONS

The 8520 PTCG allows maximum flexibility in configuration choice based upon actual job requirements in the following fields of test data recording:

1. Aircraft (fighter, bomber, transport, commercial)
2. Automotive
3. Trains
4. Helicopters
5. Medical
6. Geophysics (Earth Motion Studies)
7. Shipboard
8. Life Test Analysis

1.5 STANDARD OPTIONAL FEATURES

The Design of the Model 8520 PTCH, while allowing the user to meet his particular configuration requirements, is essentially that of the 8521 Airborne Time Code Generator (ATCG).

With Specific Standard Options (Table 1.3) Available for the 8520 PTCG the user could match his needs and attain an Airborne Configuration. These options include:

1. Shock Mounts
2. Wide Temperature Operation
3. Remote Control
4. High Stability Oscillator

TABLE 1-3

8500 SERIES STANDARD OPTIONS

MODEL	OPTION	DESCRIPTION
8520		TIME CODE GENERATOR. Portable package. Outputs IRIG B (BCD) modulated and dc level shift code in hours, minutes, and seconds. Includes display and all controls. WWV synchronization and advance/retard circuits. Operates from 12 to 50 volt dc power. Optional AC power pack. Optional built-in NiCad battery pack.
	A11E	Output IRIG E dc level shift (in place of IRIG B dc level shift). For use as slow code.
	B14	Zero warm-up, high stability oscillator. Aging rate: 2×10^{-9}/day. Stability: 5×10^{-7}/day from -40° to +55°C.
	C11	IRIG A instead of IRIG B
	C13	IRIG C instead of IRIG B
	C26	XR 3 code (250 Hz) in place of IRIG B
	C26A	XR 3 code (1 kHz in place of IRIG B

TABLE 1-3
(continued)

MODEL	OPTION	DESCRIPTION
8520	C41	IRIG A or B switch selectable
	E15	Add remote control and display connector
	L12	Plug-in ac power pack for 117/230 volt (±10%) 48-440 Hz operation (in addition to dc power operation) add 3 lbs to weight of unit.
	L14	Plug-in NiCad battery pack (unheated) including charge circuit and automatic switchover and switchback.
	L14A	Extended temperature operation (-55°C to +65°C) plug-in NiCad battery pack (heated) including charge circuit and automatic switchover and switchback.
	M13	Add Shock Mount adaptor (includes all-angle shock mount) add approximately 1-3/4" to height.
8521		TIME CODE GENERATOR. Airborne package including all-angle shock mount. 1/2 ATR size. No display or controls (except power switch) on front panel. Use Model 8585 for display and control. Unit includes extended temperature operation and zero warm-up, high stability oscillator. Operates from 12 to 50 V dc power. Optional AC power pack. Optional built-in NiCad battery pack.
	A11E	Same as 8520
	B15	Unheated Crystal Oscillator. Stability 1×10^{-5}/day (0 to 60°C)
	C11	Same as 8520
	C13	Same as 8520
	C26	Same as 8520
	C26A	Same as 8520
	C41	Same as 8520
	L12	Same as 8520
	L14	Same as 8520

TABLE 1-3
(continued)

MODEL	OPTION	
8521	L14A	Same as 8520
	M12	Portable Kit. Remove shock mount adapter and add carrying handle and feet.
	M13	Same as 8520
8580		MINATURE REMOTE TIME DISPLAY. Aircraft mount. Displays hours, minutes and seconds. Connects directly to Model 8521. For use with Model 8520, add Option E15 Model 8520.
8585		REMOTE CONTROL AND DISPLAY. Aircraft mount. Includes display and all controls for use with Model 8521. Can control Model 8520 if Option E15 is added to Model 8520.

1.6 REQUIRED FEATURE MODEL 8521 ONLY

Model 8585 Remote Control and Display Unit. Model 8585 is a companion remote control and display unit to the Model 8521 Airborne Time Code Generator. Functionally, the Remote Control and Display Unit consists of two elements: (1) a six-digit in-line remote time display assembly for displaying time corresponding to that generated by the time code generator and (2) a remote control unit which includes provisions for the following: (a) Setting the time-of-day (hours, minutes, and seconds) into the time register. (b) Resetting the time register to all zeros. (c) Run/Hold (control for stopping the count of the time register while the output code and pulse trains continue to operate). (d) Advance/Retard time rate control including rate selection. (e) Propagation delay selection control. (f) Manual control to light time display during battery operation.

CHAPTER 2

INSTALLATION

2.1 INITIAL INSPECTION

As soon as the Model 8520 PTCG is received, verify that the instrument is intact, as ordered. To insure that all Printed Circuit boards (PC boards) are firmly seated in their proper mating connector as indicated by the silkscreen on the side of chassis, the PTCG may be removed from its cover by means of loosening the 1/4-turn screw fastener at the back of the unit. If shipping damage is found, refer to the warranty (inside of this manual's back cover) and Paragraph 2.1 for repackaging instructions.

2.2 STORAGE AND RESHIPMENT

Environmental conditions during storage and reshipment should be limited as follows:

a. Maximum temperature +100°C

b. Minimum temperature -55°C

To protect your instrument during shipment or storage, use the best packaging methods available. Your SYSTRON-DONNER field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable custom packaging on short notice.

If possible, use the orignial container designed for the instrument. Otherwise; use a strong carton (350 lb. sq. inch bursting strength) or wooden box to house the instrument.

a. Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

b. Use plenty of packing material around all sides of the instrument and protect front panel with cardboard strips.

c. Seal the package with strong tape or metal bands. Mark with "DELICATE INSTRUMENT".

d. Refer to Warranty Page (inside rear cover of this manual) and check with SYSTRON-DONNER field office for shipping instructions. All correspondence should refer to an instrument by model number and the full serial number.

2.3 INSTALLATION

All Model 8520 PTCG's are shipped in a fully operable condition and require no special installation instruction except when ordered with certain optional features, (in which case) addendum sheets cover the special installation instructions.

Simply connect power cable and refer to CHAPTER 3 for Operating Instructions.

2.4 POWER REQUIREMENTS

The Model 8520 PTCG is designed for operation from a power source 12 to 50 V dc.

AC POWER PACK OPTION

Provides ac operation (in addition to dc operation) of 117/230 volts, 50 to 400 Hz. A simple internal switch change is performed for either 117 or 230 volt operation. This option adds approximately 4 pounds to the overall weight. Operation on ac or

on dc inputs above 24 volts will maintain the optional internal battery pack in a fully charged condition.

Addition:

Interconnect Requirements - Model 8585

General:

When using the Model 8585 Remote Control/Display, the interconnect cable is normally fabricated by the customer to suit his needs using the mating connectors supplied with the 8585 and the 8520 or 8521 (note that the 8520 must be ordered with option E15). This interconnect cable must conform to the following:

a) Length must not exceed 200 feet (61 meters).

b) Wire size for single conductors should be #22 AWG.

c) Connectors should be wired "pin-to-pin" e.g. pin A to pin A, B to B, etc.

d) Pin Y must be wired with shielded cable with the shield connected to pin K (signal GRD) at both ends.

e) Pin W must be wired with shielded cable with the shield connected to pin K on both ends.

f) In order to preserve the integrity of the RFI shielding of this equipment, the interconnect cable must be enclosed in shield must be connected to pin J (chassis GRD) as well as the connector shell at both ends.

FIGURE 3.1

STANDARD MODEL 8520

TIME CODE GENERATOR

CHAPTER 3

OPERATION

3.1 GENERAL

The Model 8520 PTCG is ready to operate immediately after turning on the power switch. The 1 MHz crystal controlled oscillator has an aging rate of 1 part of 10^7 per day with a stability which exceeds 1 part 10^5 per day over the operational temperature range of -20°C to +55°C. No warmup time is required within this range to achieve this stability. No preliminary adjustments or calibration procedure is necessary. It is advisable to read the following descriptions before using the PTCG.

3.2 USE OF CONTROLS, INDICATORS, AND CONNECTORS

The following paragraphs and photograph in Figure 3.1 illustrates the operation, location, and use of the Model 8520 PTCG's controls, indicators, and connectors.

3.2.1 POWER SWITCH

The power (up is ON, down is OFF) switch S1 is a locking toggle switch, which when placed in the ON position locks itself ON and the ON light is lighted. When placed in the OFF position. it locks itself OFF and the ON light is deenergized.

If the MODE CONTROL switch is in the START or RUN position when the Power switch is placed in the ON position, the PTCG will display an arbitrary time-of-day and begin counting. If in other positions of the MODE CONTROL switch when the Power switch is placed in the ON position, numerals will be illuminated

and possibly double numerals will appear but no count will occur when the Power Switch is placed in the ON position. The PTCG should be RESET, then PRESET to a desired count before proceeding.

3.2.2 BATTERY DISPLAY SWITCH

During battery operation of the PTCG (battery operation is started automatically without time loss in case external power fails), the numerical indicators are not illuminated to conserve battery life. To read the numerical indication during battery operation, hold the BATTERY DISPLAY switch S7 (a momentary switch) in the up position.

3.2.3 MODE CONTROL

Mode Control utilizes 3 separate switches to perform the Mode Control Function and allow start time accuracy to approximately 1 second. The three Mode Control switches are cited and described below:

a. PRESET S3 (FAST or SLOW) (MIN or HR) momentary toggle switch, center off.

b. RESET S4 MIN HR momentary toggle

c. START RUN MIN HR STOP S2 rotary

3.2.3.1 PRESET S3 (FAST or SLOW)

PRESET S3 (FAST or SLOW) will set either minutes or hours to a predetermined start time if S7 is in MIN or HR position and the unit previously started. FAST rate is 5 hours or minutes per second. SLOW rate is 1 hour or minute per second.

3.2.3.2 RESET S4

RESET S4 will reset the seconds, minutes, and hours accumulator to zero if S7 is in MIN or HR position independent of the previous operating MODE of the unit.

3.2.3.3 START RUN MIN HR STOP switch S7

START RUN MIN HR STOP switch S7 functions as follows:

a. START position forces manual starting of the minor counter chain and updating of the time-of-day accumulator. It permits subsequent presetting of the unit after initial application of power or after MODE switch has been in the STOP position.

b. RUN position allows external automatic starting of the minor counter by means of a momentary closure to ground derived from some external source such as the WWV 1 second tick signal.

c. MIN or HR position allows for resetting of the entire time accumulator (seconds, minutes, hours) or presetting of time in minutes or hours into the accumulator for some later start time.

The time of day accumulator is disconnected from the minor counter in the MIN or HR position causing the seconds display to remain stationary, however, the PRESETTING function requires that the minor counter chain be running to obtain the rates necessary for updating the MIN or HR accumulator with the PRESET switch. This can be accomplished in two ways. If real time is of no great importance or

a time reference signal is not available, the MODE switch should be placed in the START position then moved to the HR, MIN position. If a time reference signal is available, it is connected to the EXT SYNC (J5) input. The MODE switch is placed in the STOP position then moved to the HR position. The next occurrence of the reference signal will start the minor counter and allow presetting.

d. Stop position enables the control circuitry to stop the minor counter at the exact occurrence of the PTCG's 1 pps. When the optional REMOTE CONTROL unit is used in conjunction with the PTCG the calculated propagation delay of a received reference signal, such as WWV, can be added to the 1 pps STOP signal so that subsequent starting of the minor counter with that reference signal will compensate for the signal delay, and start the minor counter within 100 µs of the external reference signal.

3.2.4 CLOCK ADJUST

Clock adjust utilizes 2 separate switches to perform precise real time alignment of the PTCG 1 pps in synchronization with some outside 1 pps source such as WWV.

ADV RET switch S6, a momentary toggle used in conjunction with the PER SEC rotary switch S5, permits time to be added or subtracted at four decade rates from 100 microsecond per second, to 100 millisecond per second.

3.2.5 TIME DISPLAY

Time is displayed in hours, minutes, and seconds by means of a horizontal array of six ultra-long-life cold cathode numerical display tubes, mounted behind a polarized filter for reduction of glare. Normal maximum viewing distance for the 0.5 inch high neon read characters is 24 feet.

3.2.6 MOD CODE J3

The MOD CODE BNC connector (J3) is the output connector for the modulated serial Binary Coded Decimal (BCD) code representing time in hours, minutes, and seconds with a carrier frequency of (1 kHz IRIG B) or (1 kHz or 250 Hz XR 3). The MARK output level is adjustable from 0 to 10 V peak-to-peak from a low impedance 15 mA current source. The Modulation ratio MARK to SPACE is adjustable from 2:1 to 6:1 nominally set to 3:1.

3.2.7 DC CODE J4

The Output Level Shift Code J4 (dc CODE) dc level for IRIG B or XR 3 BCD code is 0 (±0.4) volts to +5 volts clamped into a 1 kΩ load. Positive going edge is (on time).

3.2.8 PULSE RATE OUTPUTS J6 J7 J8

Three simultaneous pulse trains are provided at rates of 1 k pps J6, 100 pps J7, and 1 pps J8 at their individual BNC connectors. Output level for each is 0 ±0.4 V dc to +5 V dc peak from a 5 mA current source. Rise time is approximately 0.5 microseconds.

3.2.9 EXT SYNC J5

The EXT SYNC BNC J5 connector is the input from some external

1 pps time reference signal such as WWV tick envelope for synchronization of the PTCG (see 3.2.4 and 3.3.6).

3.3 OPERATION

A step by step operating procedure is outlined in the following paragraphs.

3.3.1 TURN ON PROCEDURE

a. Insure that dc power is supplied correctly to POWER INPUT connector J1; i.e., +28 V dc measured between pin C to A of J1's mating connector. Check that the fuse F1 is installed and of proper value: 2 amperes (2A 3AG).

b. Place power switch in the up (ON) position.

3.3.2 RESET PROCEDURE

The 8520 cannot be reset with the MODE switch S2 in positions other than HR or MIN.

a. Place MODE switch S7 in HR or MIN.

b. Place the RESET switch S4 in the up position momentarily. The display will now indicate all zeros and all zeros are set into the seconds, minutes, and hours accumulator for a specific future start time.

3.3.3 PRESET TIME PROCEDURE

a. Set S2 Rotary switch to START position, then to HR position.

b. Reset (see 3.3.2) to clear the arbitrary numerals appearing on the 6 digit time display.

c. Place S3 PRESET momentary toggle to FAST or SLOW and set in desired time in hours.

d. Set S2 Rotary switch to the MIN position.

e. Place S3 PRESET momentary toggle to FAST or SLOW and set in the desired time in minutes. The time displayed is also the time set into the minutes and hours accumulators.

f. At the time of interest, move S2 to the RUN position.

3.3.4 STOP PROCEDURE

A STOP procedure is necessary in order that the TIME BASE/MINOR COUNTER register may be started "On Time" by being stopped in a known preset condition (see 3.2.3.3 d). STOP is effected merely by placing MODE CONTROL S2 in the STOP position.

The 8520 PTCG with NO Remote Control unit will stop with 000.00 milliseconds stored in the register, therefore, it will start "On Time" from an outside "On Time" electronic reference signal and provide an update signal to the time of day accumulator exactly one second later.

The 8520 PTCG operating with a Remote Control unit will stop with the time PRESENT into the propagation delay switches of the Remote unit stored in the TIME BASE/MINOR COUNTER register. A SYNC signal with a known delay up to 99.9 milliseconds can then be used to start the PTCG "On Time".

3.3.5 MANUAL START PROCEDURE

a. Place the MODE switch (S7) to the START position at the

moment the time equals the preset time. Time will now accumulate from this moment and the display will advance once each second.

b. After a manual start, the PTCG may be adjusted as outlined in Paragraph 3.3.7.

3.3.6 AUTOMATIC START PROCEDURE

The following procedure is used to synchronize the internal 1 pps with an external WWV signal. Any WWV signal adjusted to an amplitude of approximately 5 V peak-to-peak may be used. The correct amplitude for signals having large noise content will have to be determined by experiment i.e., viewing the output of A7 Pin A/15 and externally adjusting the WWV input for a 1 pps pulse output of the required amplitude.

a. Set the MODE CONTROL switch to STOP, and then to either HRs or MINs.

b. Connect the external 1 pps reference to EXT SYNC connector (J5).

c. Set the MODE CONTROL switch (S2) to the RUN position.

d. The internal 1 pps reference of the 8520 PTCG is now synchronized with external 1 pps reference and updated time is being displayed. The external reference may now be removed.

NOTE

Although the internal reference is now "on time", the clock has not been set to the correct time-of-day. This may be accomplished by the procedure outlined in Paragraph 3.3.3. As long as the MODE CONTROL switch (S2) is not placed in STOP position, this procedure will not cause loss of internal reference synchronism, since, although the readout is stopped, the internal 1 pps reference is still being generated and maintains the sync which has been established.

3.3.7 SYNCHRONIZATION PROCEDURE

In order to precisely sychronize the 8520 PTCG, the following test equipment is required. Oscilloscope Tektronix Model 535 or equal, Precision Time Source WWV, Laboratory Clock, etc. Once the 8520 PTCG has been started, it may be desirable to synchronize, particularly, if the Manual Start procedure has been used. The following procedure may be used and will not require resetting the clock.

1. Connect a time standard such as WWV to one vertical axis input of a dual trace oscilloscope.
2. Connect the 1 pps output from the 8520 PTCG connector (J8) to the second vertical axis input of the scope.
3. Ascertain that the PTCG is displaying time within 1 second of the correct time as received from the reference signal. This may be done by a visual check of the laboratory clock or by monitoring the audio WWV announcement.
4. Superimpose the two traces on the oscilloscope and determine whether the internal 1 pps signal is leading

lagging the external 1 pps reference.

5. Set the CLOCK ADJUST PER SEC switch (S5) to a rate that will correct for the difference between the two pulses in a few seconds.
6. If the internal 1 pps is lagging, place the ADV/RET switch (S6) in ADV position and hold until the leading edge of both pulses are perfectly coincident. If the internal 1 pps pulse is leading, use, the RET position of S6. In either case, the switch will return to the neutral position when released.
7. For a more exact synchronization, expand the time base on the oscilloscope and repeat the above procedure using a slower Rate/Second setting of S5.

CHAPTER 4

MAINTENANCE AND CALIBRATION

4.1 FACTORY SERVICE

When the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns when necessary. Address all inquiries on operation or application to your nearest sales representatives, or to:

Sales Manager, SYSTRON-DONNER CORP.
888 Galindo Street
Concord, California 94520

Specify both model and complete serial number in all correspondences.

4.2 ROUTINE MAINTENANCE

A regular program for routine maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1. Disconnect power and remove the cover.
2. Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.
3. Check for physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a printed circuit board contains integrated circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

4. Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.
5. If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and a low pressure stream of air to remove the foreign material.

CAUTION

Do not clean PC boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacum cleaner device must not be used on small internal components.

6. Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints, and other foreign material.
7. Replace the cover and reconnect power. Perform the Operational Test and Calibration Procedure (Paragraph 4.6). If performance does not match or exceed the specifications listed in Chapter I of this manual, corrective maintenance is in order.

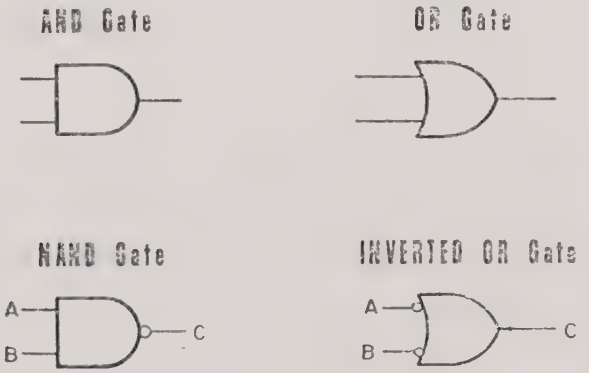
4.3 PRINTED-CIRCUIT BOARD REPAIR

To remove a part on a printed-circuit board, cut the leads of the part near the lead holes. Using a low power (50 watts of less) soldering iron, apply heat sparingly to each cut lead. As soon as the solder melts, slip the lead from the hole and clean the hole with a toothpick. Clean the board surfaces with isopropyl

alchol. Form the tinned leads of the replacement part and insert in cleaned holes, trimming the leads to extend 1/16 inch beyond the back surface of the board. Only 63/37 solder with a maximum diameter of 1/16 inch should be used. Solder the leads to the board and use a hemostat, long-nosed pliers, or other heat sink on the leads of all semiconductor devices and quarter-watt resistors. Allow the soldered junction to cool before removing the heat sink.

4.4 LOGIC FUNCTIONS

The logic symbols and functions, as used in the Model 8520/8521, are described in the following paragraph. Truth tables and detailed explanations are given where necessary in order to assist qualified maintenance personnel in the repair and upkeep of the instrument.



The NAND Gate and the INVERTED OR Gate have the same truth tables.

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

INVERTED AND Gate

The NOR Gate and the INVERTED AND Gate have the same truth tables.

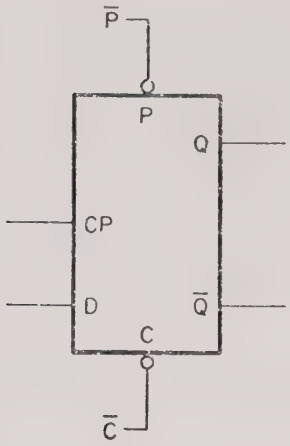
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

DOT AND

DOT OR

In some configurations it is possible to perform the AND and OR function simply by tying the outputs of certain gates together. These functions are called DOT AND and DOT OR functions. The nature of the signals fed to the "DOT" determines whether the function is AND or OR. When several "DOTS" are present on a single line, the AND or OR symbol is used only once.

D-TYPE Flip-Flop



(1) Q assumes the state of the D input on the positive transition of the clock (CP) input.

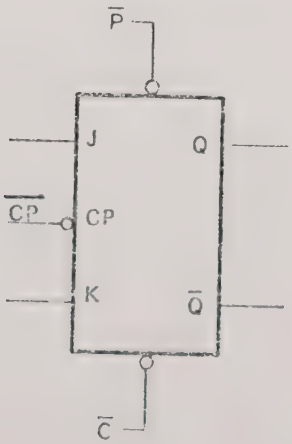
(2) The D input is locked out when the clock input is positive.

(3) $\overline{P}$ and $\overline{C}$ override all other inputs.

(4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.

(5) At a preset condition, Q is a Logic 1. At clear condition, Q is a Logic 0.

JK-TYPE Flip-Flop



4.5 JK-TYPE FLIP-FLOP

(1) If J and K are both at Logic 0 when the clock input ($\overline{CP}$) assumes a Logic 0 state there is no change in the output.

(2) If K is a Logic 1, Q will assume a Logic 0 when $\overline{CP}$ goes to Logic 0.

(3) If J is a Logic 1, Q will assume a Logic 1 when $\overline{CP}$ goes to Logic 0.

(4) If J and K are both at Logic 1 the flip-flop will change state when the $\overline{CP}$ goes Logic 0.

(5) The J and K inputs are locked out then the clock input is Logic 0.

(6) $\overline{P}$ and $\overline{C}$ override all other inputs.

(7) If $\overline{P}$ and $\overline{C}$ are both at Logic 0 the Q and $\overline{Q}$ outputs are both at Logic 1.

(8) At the preset condition, Q is a Logic 1. At a clear condition Q is a logic 0.

4.6 OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the technician to isolate the trouble to a particular circuit card.

When the trouble is isolated to a card description in Chapter 6 will facilitate repair.

WARNING

DANGEROUS HIGH VOLTAGES ARE PRESENT IN THE POWER SUPPLY AND DISPLAY CIRCUITS OF THIS EQUIPMENT. USE CAUTION AT ALL TIMES WHEN THE PROTECTIVE COVERS ARE REMOVED.

4.6.1 RECOMMENDED TEST EQUIPMENT

The following test equipment or equivalent is recommended for use in servicing the Model 8520/8521.

MODEL	MANUFACTURER	DESCRIPTION
535A	TEKTRONIX, INC.	Oscilloscope, 15 MHz Bandwith sweeps from 0.1 microseconds/cm to 5 sec/cm.
CA	TEKTRONIX, INC.	Dual-Trace Calibrated preamp for 535A scope, 0.05 volts/cm to 20 volts/cm.
P6000	TEKTRONIX, INC.	Probe, 10:1 Attenuation Ratio, 12 pf of capacitance.
9000	SYSTRON-DONNER CORPORATION	VOM, 10 MΩ input impedance, ±0.1% accuracy.

In addition to the equipment listed above, a receiver capable of receiving WWV is required to accurately check the WWV sync circuit. To test the ADVANCE/RETARD system (especially the slower rates), another time code generator should serve as a 1 pps reference. Lacking another TCG, any reliable 1 pps source may be used.

4.6.2 POWER SUPPLY Dwg. # 31248-7-1 and 31214-7-2

The voltage checks listed below will insure the correct operation of the power supply assuming that the 12 V adjust is properly set (refer to paragraph 4.6.3).

(1) Insure the presence of +200 V dc ±20% on Pin B/16 of A8.

(2) Insure the presence of +5 V dc ±0.5 V on the +5 V buss, (on the underside of the chassis with many red wires on it).

4.6.3 SWITCHING REGULATOR Dwg. #31248-7-1 and 31214-7-2

The switching regulator maintains 12 V dc for the DC to DC converter. The voltage is adjusted by monitoring the 5 V buss and setting R14 to give +5 V dc ±0.5 V. This is the only adjustment in the power supply.

4.6.4 AC SUPPLY Dwg.#31151-7-1

This plug-in unit has provision for using either 115 or 230 V ac input. Be certain that the selector switch is set correctly for the line voltage being used.

4.6.5 TIME BASE AND OSCILLATOR Dwg. #31209-7-2

The accuracy of the oscillator may be determined, relative to a frequency standard, by observing the rate of drift of an oscilloscope pattern as shown in Figure 4.1, the oscillator accuracy test diagram.

If the pattern moves to the right, the frequency of the oscillator under test is lower than that of the frequency standard; if the pattern moves to the left, the frequency under test is too high.

To check oscillator frequency (not stability):

(1) Trigger the oscilloscope externally with the 1 MHz internal oscillator of the 8520/8521.

(2) Connect a 1 MHz frequency from an external standard to the vertical input of the oscilloscope.

(3) Set the oscilloscope sweep time to 0.1 μsec/cm and adjust the controls to obtain a presentation of a 5 V peak-to-peak waveform.

(4) Horizontal drift of the oscilloscope display in cm/sec is the difference from the standard frequency in parts/10^7. If necessary adjust the oscillator.

(5) To adjust the standard oscillator vary the setting of C9 on the TIME BASE, ADV/RET SYNCHRONIZER card. To adjust the high stability oscillator, remove the screw covering the adjustment capacitor and vary the setting.

(6) Verify the presence of a 100 k pps signal at Pin B/18 and 500 k pps at Pin B/17.

TABLE 4-1

OSCILLATOR ACCURACY

Drift	Accuracy
1 cm/0.1 sec	1 part in 10^6 (10 Hz)
1 cm/sec	1 part in 10^7 (1.0 Hz)
1 cm/10 sec	1 part in 10^8 (0.1 Hz)

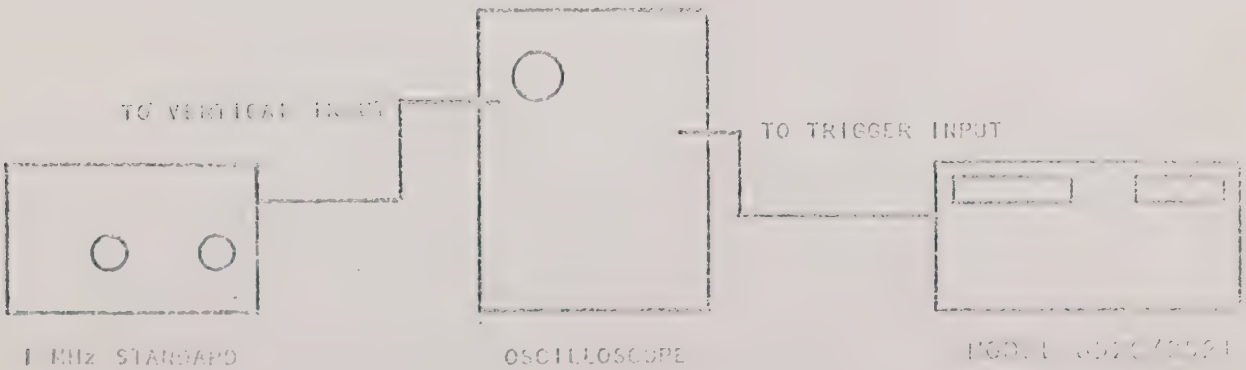
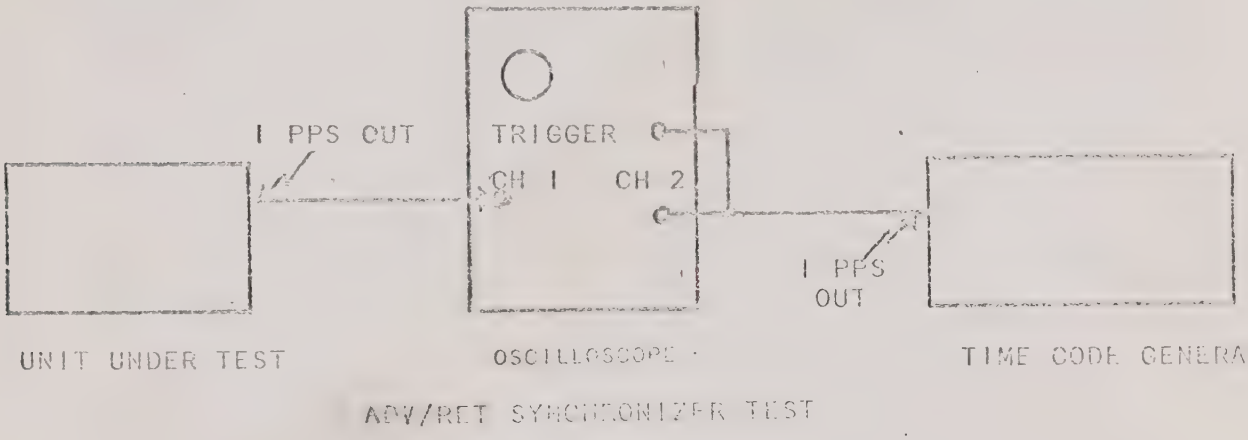


FIGURE 4.1
OSCILLATOR ACCURACY TEST

4.6.6 ADV/RET SYNCHRONIZER Dwg. #31209-7-2

To test the operation of this circuit connect on the oscilloscope as shown in Figure 4-2. Adjust the time base as required to give sufficient resolution for each ADV/RET rate selected.



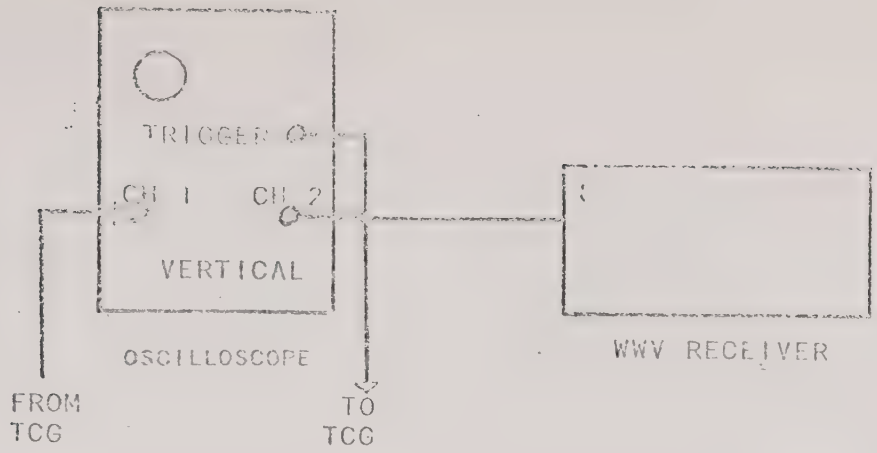
ADV/RET SYNCHRONIZER TEST

FIGURE 4.2

With both generators operating, there will be some arbitrary time difference between the pulse trains. Starting with the fastest ADV/RET rate available, verify that the pulse train from the unit under test shifts (right or left depending on whether ADV or RET is selected) the proper time increment each second. Repeat this procedure for each of the other rates. It will be necessary to bring the pulse trains into closer coincidence for each slower rate and to increase the time base speed.

4.6.7 CONTROL, INPUT/OUTPUT

To test the WWV sync circuit connect the oscilloscope as shown in Figure 4-3. Sync the scope to show the 5 cycles of 1 kHz which comprise the 1 second "TICK".



WWV SYNC CIRCUIT TEST
FIGURE 4.3

Monitor the output of the WWV sync circuit on either pin B/22 or A/15 and verify that a pulse is produced once for each burst of 1 kHz.

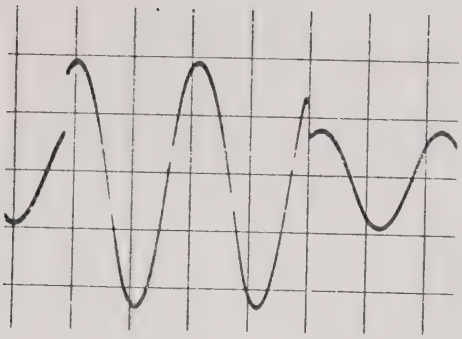
The code output circuit contains three adjustments. These control the shaper tuning, mark to space ratio, and nominal output amplitude.

(1) Adjust the tune (R13) control for maximum AC signal at the MOD CODE output connector

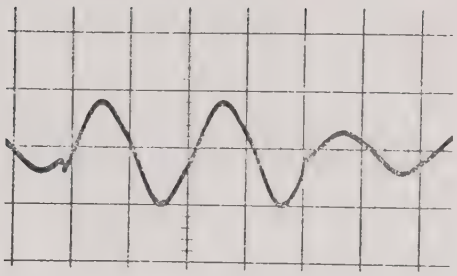
(2) Adjust the MOD (R25) control for a nominal 3 V peak-to-peak output of the large cycle signal.

(3) Adjust the ratio (R22) control for a 3:1 modulation ratio.

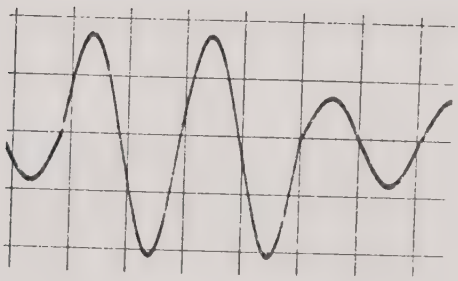
(4) Readjust the tune (R13) control until the junction point of the large and small cycles has a minimum of distortion. (See Figure 4-4).



Incorrect
Adjust Tune Control CW



Incorrect
Adjust Tune Control CCW



Correct

FIGURE 4.4
Tune Control Adjustment

CHAPTER 5

OVERALL FUNCTIONAL DESCRIPTION

5.1 TIME BASE ADV/RET SYNCHRONIZER

A stable 1 MHz signal is produced by the oscillator section of this card. This 1 MHz signal is divided down to 500 kHz and 100 kHz for use by the minor counters.

The ADV/RET SYNCHRONIZER allows setting the time code generator into coincidence with a standard time reference. The time may be shifted at one of six rates, 1 µs/sec to 100 ms/sec, and either advanced or retarded. Advance is accomplished by adding pulses into the minor counters, retard by deleting pulses.

5.2 TIME BASE, MINOR COUNTERS

A five decade counter divides the incoming 100 k·pps signal down to 1 pps. The decades are arranged so that the first two are reset independentiy of the last three to permit setting of propagation delay. The EXT RESET signal resets the last three counters RESET (and START/STOP) of the first two counters is controlled by the MANUAL or AUTO START and STOP LINES. All outputs of the decades are buffered.

Three sets of gates decode the minor counter outputs to provide square waves at 10 kHz, 1 kHz, and 100 Hz.

5.3 TIME-of-DAY ACCUMULATOR

The accumulator card stores the time information and is updated by the 1 pps signal from the minor counters. In the preset condition the hours, minutes, and seconds portions of the accumulator are electrically separated so that each portion can be separately preset to a desired condition. Circuitry is included to serially preset the entire accumulator chain when used with a remote control box. The parallel BCD outputs of the accumulator, buffered to prevent disturbance from external effects, are used to drive the internal display tubes and when equipped with the proper option used to drive peripheral equipment such as computors and/or remote time displays.

5.4 CODE GENERATOR

The code generator card accepts a rate input of 10X the bit rate of the desired serial code plus the BCD outputs of the time accumulator and generates the complete serial dc code format. A number of digitally controlled switches serialize the BCD time information which is further gated by timing signal to produce a pulse width modulated output.

5.5 DUAL SHAPER MODULATOR

This card contains circuitry to shape either of two input square waves to produce coherent sine waves used as carriers for the modulated serial output codes. Generally, this card is used when it is required to generate more than one code, and is only partially assembled when a single code is generated. Additional circuitry is provided to buffer the output pulse rates and to process additional control signals.

CHAPTER 6

CIRCUIT DESCRIPTION AND ILLUSTRATIONS

All plug-in modules are designed so that the card will only fit into position if it is correctly aligned; however, caution must be exercised to insure that a card is installed in the correct card slot. Latching handles on all cards are numbered to facilitate correct installation.

CAUTION

When mounting a card on the extender board it is possible to install the card backwards which will result in serious damage.

6.1 POWER SUPPLY Dwg. #31248-7-1, 31214-7-2, 31151-7-1 C, 31183-7-2)

General

The power supply provides four voltage from a switching regulator controlled dc to dc converter. The voltages are +15, -15, +5 and +200 V dc. The input to the supply is from one of three sources: A built-in (Optional) ac power supply, an external dc voltage (28 V nominal, 12 to 50 V dc) or a built-in (Optional) rechargeable battery pack. Provision is made for automatic, instantaneous changeover to the internal batteries should external power fail.

Input and Control Circuit (Refer to Dwg. # 31248-7-1)

The external dc power source enters the unit through a PI section filter network #31200-4-1. Diodes CR5 and CR15 allow operating the optional battery heater and the display control relay at all times when dc power is applied or when the ac supply is on. Diodes CR6 and CR7 form a switch to automatically connect the batteries whenever the input voltage is below the battery voltage. Resistor R4 and diode CR8 permit battery charging when the unit is turned on. Relay K1 controls the 200 V for the illuminated display when the unit is operating. Its primary function is to disconnect the display from the power supply during battery operation to conserve power. The "BATTERY DISPLAY" switch permits turning on the display, momentarily. When the unit is operating from either the ac supply or an external dc voltage, K1 will be held on by diode CR15, keeping the display on. Resistor R6 is used to prevent K1 from energizing when the battery voltage drops below 12 V. In this way, the "BATTERY DISPLAY" switch serves as a "near-end-of-operation" test

for the battery; i.e. when the display does not light with the switch depressed, the battery is nearing its minimum voltage point. The ac supply is diode coupled to the input circuit and automatically powers the unit when turned on.

AC Power Supply - Optional (Dwg. #31151-7-1 C)

The ac power supply accepts 115/230 V (selected internally with a switch), through a line filter, and delivers 28 V dc through two diode isolated outputs. Diodes CR1 and CR2 form a full wave rectifier, diodes CR3 and CR4 are used to isolate the supply from the other voltage sources in the unit.

Switching Regulator (Dwg. #31214-7-2)

The switching regulator accepts an input of 12 to 50 V dc and supplies a regulated voltage of approximately 12 V to the dc to dc converter. Refer to Dwg. #31214-7-2. Transistor Q5, zener diode CR4, and potentiometer R14 form an adjustable current source. The current generated flows through R12, producing a constant voltage across the resistor. In this way the voltage at Q4 base follows the regulated voltage and the offset is adjustable. The voltage is applied to the Schmitt Trigger (Q2 and Q3) through emitter follower Q4 and zener diode CR3. The Schmitt Trigger causes Q1 to conduct when the voltage drops below the set point. This causes Q1 (on Dwg. #31248-7-1) to conduct, producing a pulse of voltage. The voltage pulse is applied to capacitors C3, C4, and C7 (Dwg. #31214-7-2) through inductor L1 (Dwg. #31248-7-1). When the voltage reaches the set point, the Schmitt Trigger turns off, terminating the voltage pulse. A series of pulses is produced to keep the voltage on the capacitors at the set point. The network composed of L1, C3, C4, and C7

smoothes the pulses to give a steady voltage. Zener diode CR13 is used to shut off the regulator when the input voltage is less than 12 V.

DC to DC Converter

The voltage from the switching regulator is applied to the center point of the collector winding of T1 (Dwg. #21248-7-1). Bias for the base winding center point is provided by R7 and R17 (on Dwg. # 31214-7-2). Q2 and Q3 (Dwg. #21248-7-1), along with R1 form a free-running oscillator which produces square wave ac on the three output windings. One winding supplies +5 V through a full wave rectifier, CR11, CR12 (Dwg. #21248-7-1) another 200 V through a full wave bridge rectifier CR9-12 (Dwg. #21790-4-1) and the third +15 V and -15 V through full wave rectifiers CR5, CR8, and CR6, CR7.

Battery Heater - Optional Dwg. # 31183-7-2)

The battery heater allows operation down to -55°C. Thermistor RT1 senses the battery temperature by changing its resistance with changes in temperature. Zener diode CR1 porvides a regulated voltage for the input voltage divider and the Schmitt Trigger. The voltage change at Q1 base is coupled by Q1 (as an emitter follower) into the Schmitt Trigger Q2, Q3. A decrease in temperature causes RT1 to increase resistance, thereby increasing the voltage at Q1 emitter. This causes Q3 to turn on, turning on Q4, Q5, and thus the heater.

PARTS LIST

BATTERY PACK P/L 31144-7-1

Ref.	Description	S-D Part No.
	Assembly	31144-4-1
	Schematic	31144-7-1
BT1,2	Battery (Gulton 8 V 0.750)	BT0002
J9	Connector, Winch MRE5-3SN7HVL	J0573
RT1	Thermistor, GE 1D101	

TRANSFORMER BRACKET ASSEMBLY P/L 21790-7-1

	Assembly	21790-4-1
	Schematic	21790-7-1
C5	Capacitor, 0.01 µf	C0341
CR9	Diode, IN4005	CR0284
CR10	Diode, IN4002	CR0276
CR11,12	Diode, IN1201A	CR0295
K1	Relay, Babcock BR8-600-B3-26 V	
L1	Inductor, 4 mh, TT2320	31182-1-1
Q1-3	Transistor, 2N3715	Q0223
R7	Resistor, 56 Ω, 1/4 W	R1554
R8	Resistor, 250 Ω, 5 W	R2360
	#6-32 Float Pem	H0811
	Standoff	E0098
	Standoff	E0131

COMPONENT BKT. DC POWER SUPPLY P/L 31201-7-1

	Assembly	31201-4-1
	Schematic	31201-7-1
C3	Capacitor, 110 µf, 50 V (39 D)	C1103
C4,5	Capacitor, 0.33 µf, 400 V	C1131
CR5,8,14,15	Diode, IN4005	CR0284
CR6,7	Diode, IN1201A	CR0295
R3	Resistor, 220 k Ω, 1/2 W	R0264

PARTS LIST (cont)

Ref.	Description	S-D Part No.
R4	Resistor, 100 Ω, 5 W	R1674
R5	Resistor, 560 Ω, 1 W	R1668
R6	Resistor, 220 Ω, 1/4 W	R0760

LINE FILTER ASSEMBLY P/L 31200-7-1

	Capacitor, 0.1 µf, ±20%, 50 V	C0781
	Inductor, Miller 5248, 68 µh, 2A	L0151

SWITCHING REGULATOR P/L 31214-7-2

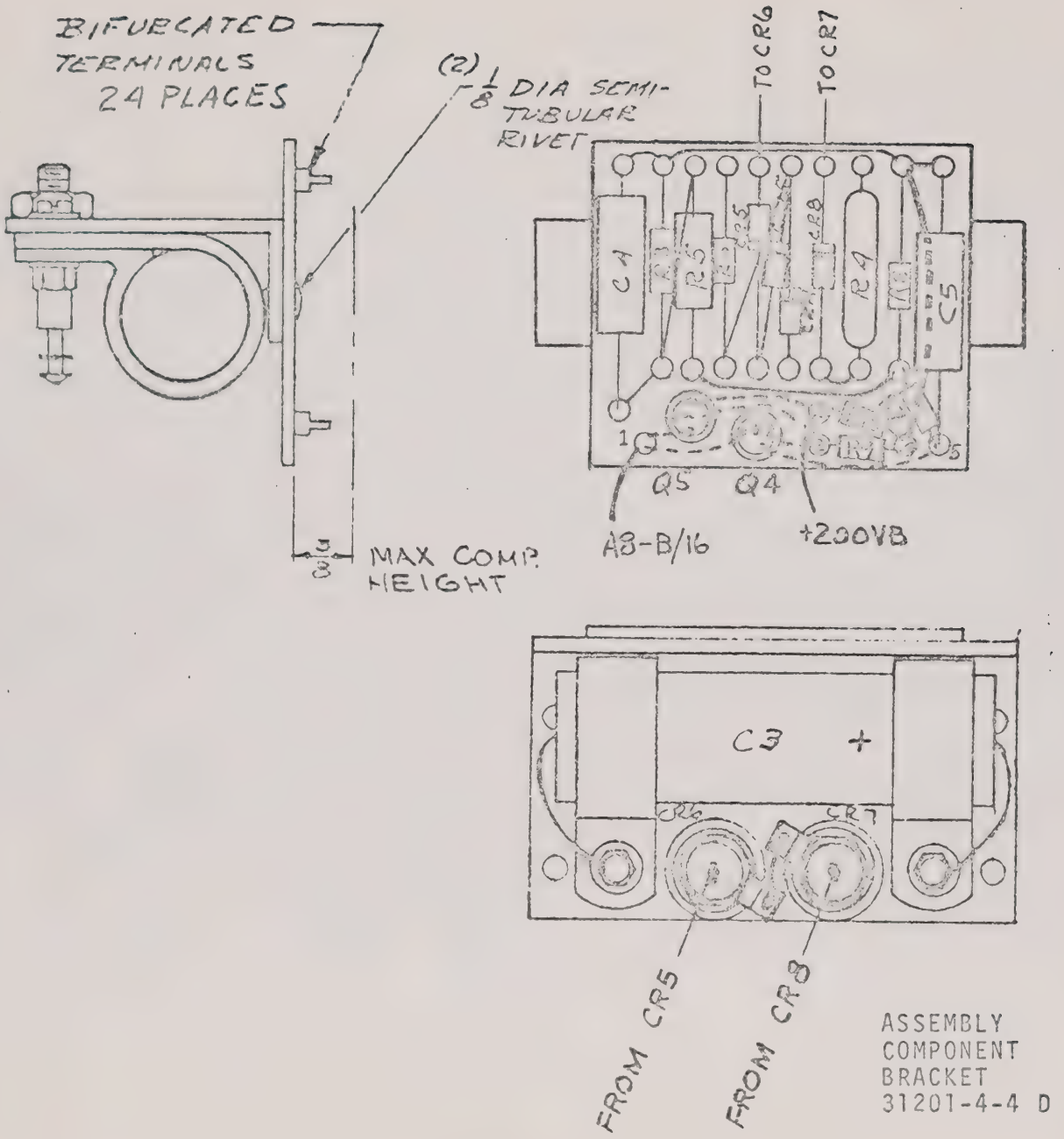
C1	Capacitor, 1 µf, 20 V	C0524
C2	Capacitor, 150 pf	C0537
C3,4,7	Capacitor, 150 µf, 15 V	C1026
C5	Capacitor, 0.1 µf, 200 V	C0987
C6,8	Capacitor, 0.01, Ceramic Disc	C0341
C9,10	Capacitor, 47 µf, 35 V	C0982
C11	Capacitor, 0.33 µf, 400 V, Electron, D4-334	C1131
CR1	Diode, IN4739	CR0340
CR2	Diode, IN4002	CR0276
CR3,4	Diode, IN702	CR0126
CR5-12	Diode, IN4005	CR0284
CR13	Diode, IN756A	CR0346
R1	Resistor, 470 Ω, 2 W, 5%, CC	R2082
R2	Resistor, 4.7 k Ω, 1/4 W, 5% CC	R0892
R3	Resistor, 470 Ω, 1/4 W, 5% CC	R1044
R4	Resistor, 30 Ω, 1/4 W, 5%, CC	R1549
R5	Resistor, 1 k Ω, 1/4 W, 5%, CC	R0765
R6,7	Resistor, 1.8 k Ω, 1/4 W, 5% CC	R0959
R8	Resistor, 1.2 k Ω, 1/4 W, 5% CC	R0809
R9,11	Resistor, 2.2 k Ω, 1/4 W, 5% CC	R0749
R10	Resistor, 150 Ω, 1/4 W, 5%, CC	R0983

PARTS LIST (cont)

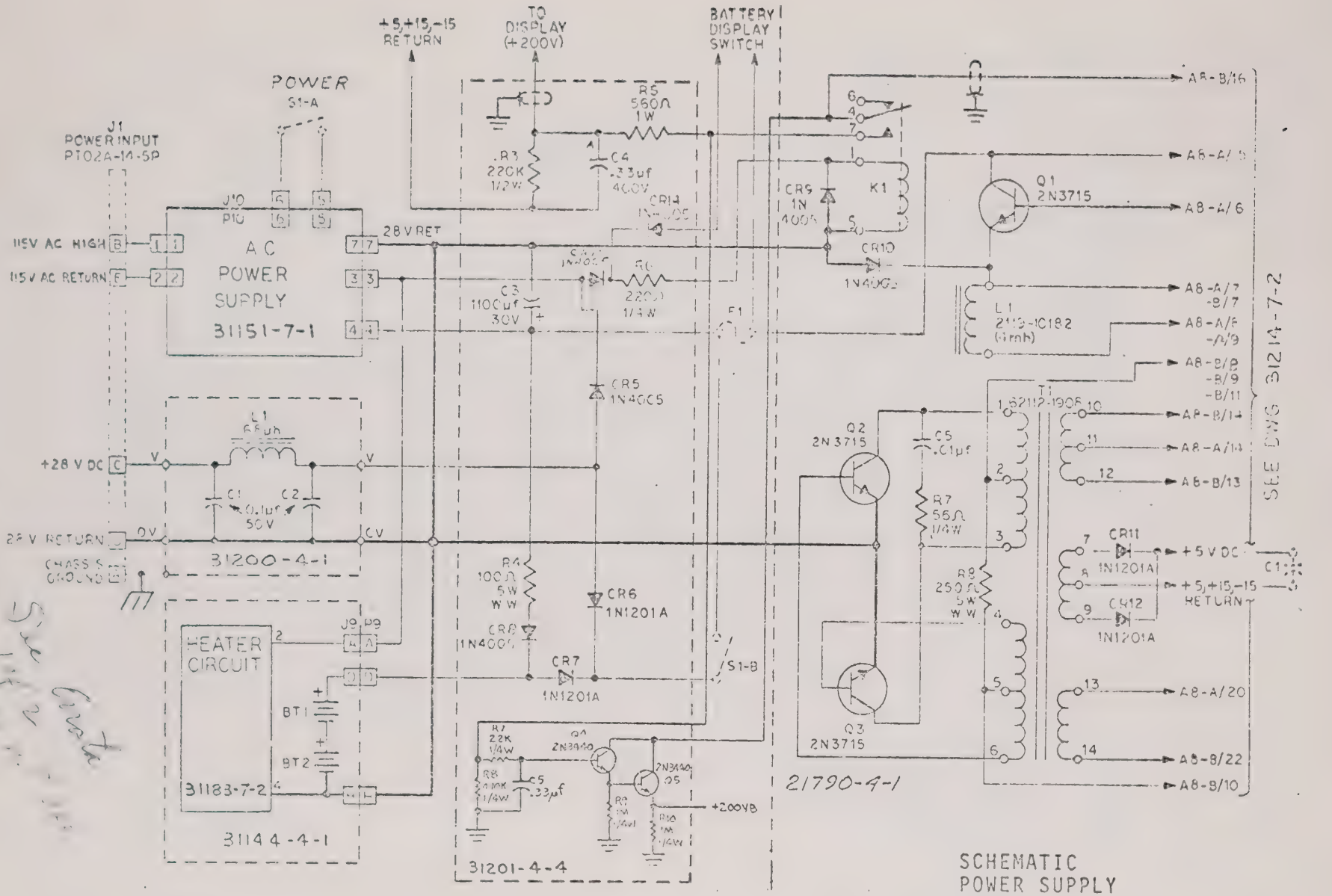
Ref.	Description	S-D Part No.
R12,15	Resistor, 5.6 k Ω, 1/4 W, 5%, CC	R0821
R14	Resistor, 5 k Ω, Variable WW (Bourns)	R2335
R16	Resistor, 56 Ω, 1/4 W, 5%, CC	R1554
R17	Resistor, 30 Ω, 2 W, 5%, CC	R2267
R18	Resistor, 220 k Ω, 1/4 W, 5%, CC	R0264
R13	Resistor, 1.5 k Ω, 1/4 W, 5%, CC	R0783
Q1	Transistor, 2N2905	Q0259
Q2-5	Transistor, 2N2222	Q0116

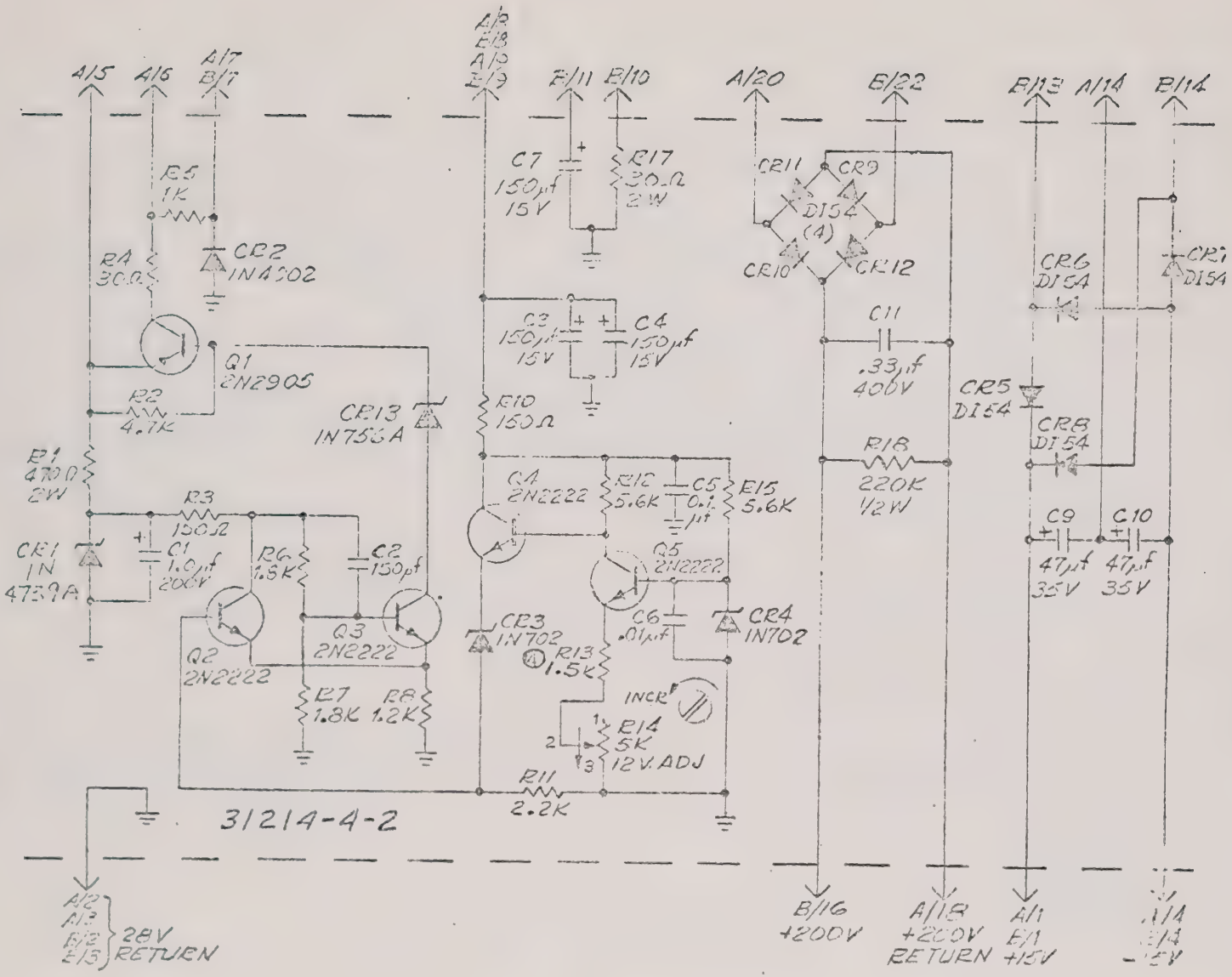
AC POWER SUPPLY

C1	Capacitor, 1100 µf, 50 V SPR39D	C1103
CR1,2,4	Diode, IN1201A	CR0295
CR3	Diode, IN4002	CR0276
F2	Fuse, 1/2 H, 3AG, S10 B10	F0012
P10	Connector, Amph 264100-8P	J0557
XF2	Fuse Holder	X0034
Z1	Line Filter, GF1162	L0038
	Terminal	E0098



ASSEMBLY
COMPONENT
BRACKET
31201-4-4 D

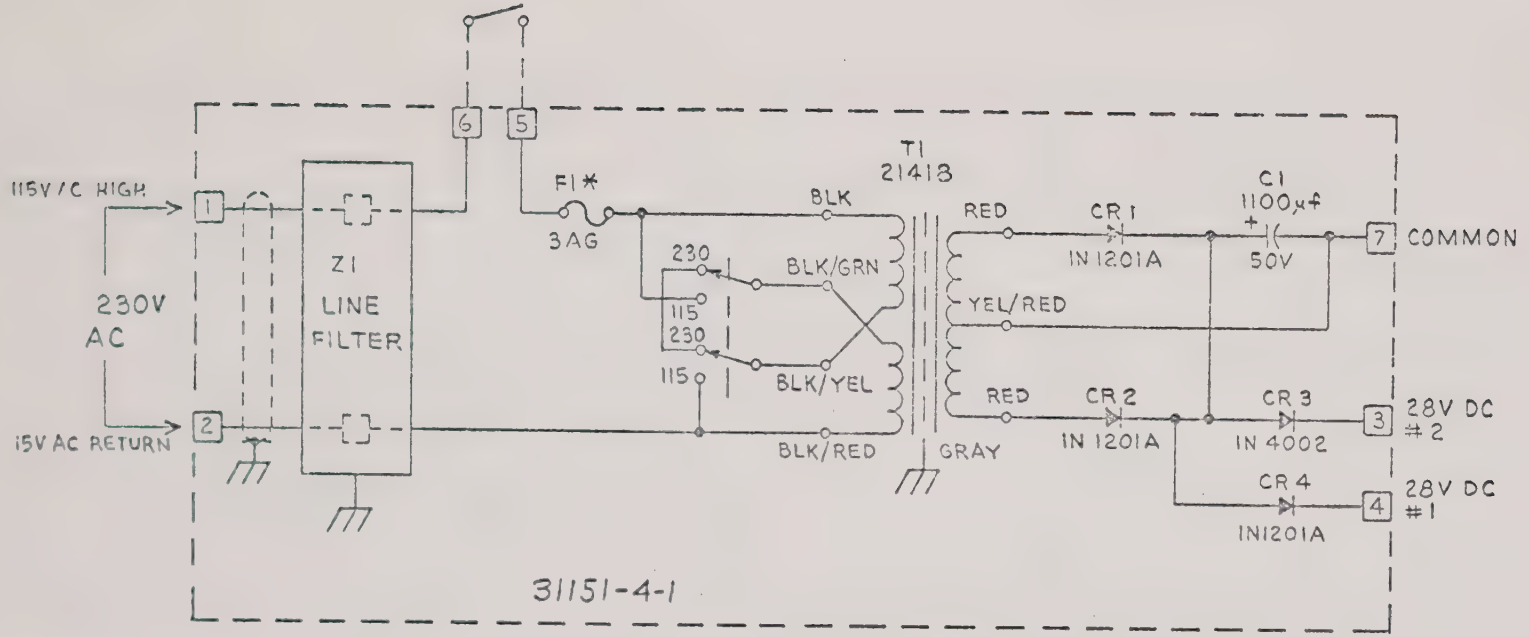

+5,+15,-15 RETURN
TO DISPLAY (+200V)
BATTERY DISPLAY SWITCH
POWER S1-A
J1 POWER INPUT PT02A-14-5P
J10 P10
115V AC HIGH
115V AC RETURN
AC POWER SUPPLY 31151-7-1
28V RET
R5 560Ω 1W
R3 220K 1/2W
C4 .33uf 400V
CR4 1N4005
CR9 1N 4005
K1
CR10 1N4002
Q1 2N3715
L1 2119-10182 (6mh)
C3 1100uf 30V
R6 220Ω 1/4W
F1
CR5 1N4005
+28 V DC
28 V RETURN
CHASS S GROUND
L1 68uh
C1 C2 .01uf 50V
31200-4-1
R4 100Ω 5W WW
CR8 1N4004
CR6 1N1201A
CR7 1N1201A
S1-B
HEATER CIRCUIT
J9, P9
BT1
BT2
31183-7-2
31144-4-1
R7 22K 1/4W
Q4 2N3440
R8 2.10K 1/4W
C5 .33μf
Q5 2N3440
R9 1M 1/4W
R10 1M 1/4W
+200VB
31201-4-4
Q2 2N3715
Q3 2N3715
C5 .01μf
R7 56Ω 1/4W
R8 250Ω 5W WW
T1 62112-1905
CR11 1N1201A
CR12 1N1201A
+5 V DC
+5,+15,-15 RETURN
C1
21790-4-1
A8-B/16
A8-A/5
A8-A/6
A8-A/7
-B/7
A8-A/8
-A/9
A8-B/8
-B/9
-B/11
A8-B/14
A8-A/14
A8-B/13
A8-A/20
A8-B/22
A8-B/10
SEE DWG 31214-7-2
SCHEMATIC
POWER SUPPLY
31248-7-1



NOTES

1. ALL RESISTORS ARE COMP. CARB. ± 5% 1/4 W

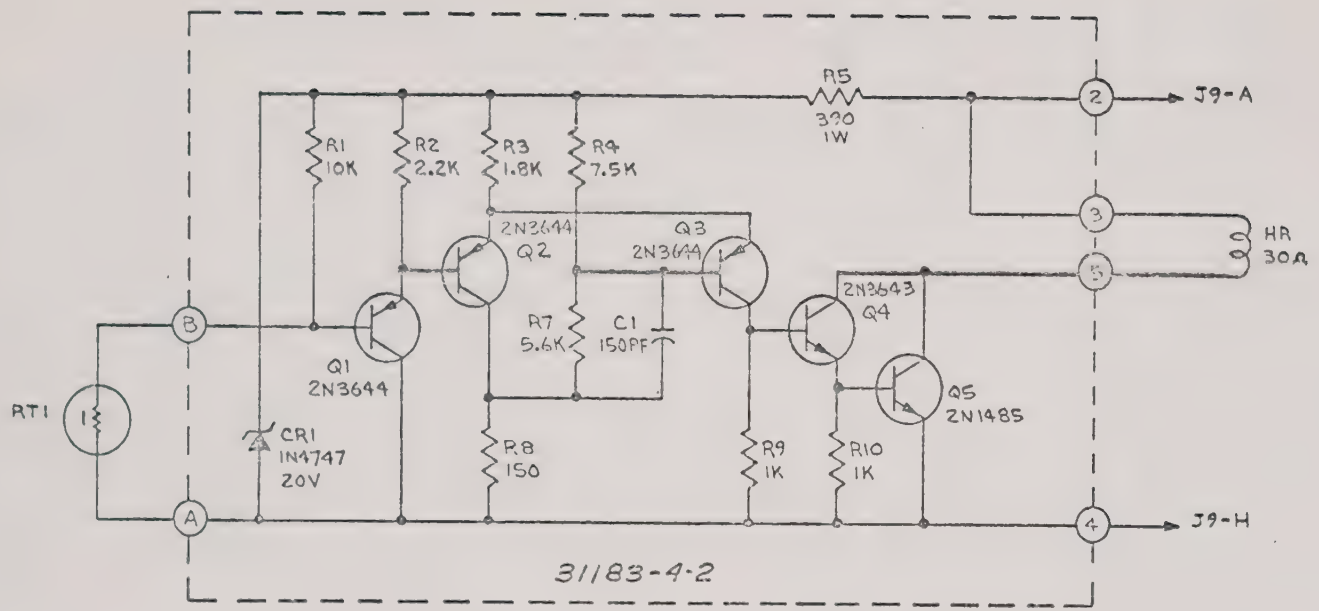
SCHEMATIC
SWITCHING
REGULATOR
31214-7-2 A



nº = PINS OF J10, "AMPHENOL #26-4200-8P, & THE MATE P10, "#26-4200-8S"

F1 = 1/2 A FOR 115V OPERATION.
1/4 A FOR 230V OPERATION.

SCHEMATIC
AC POWER
SUPPLY
31151-7-1



NOTE: (UNLESS OTHERWISE SPECIFIED)
1. RESISTORS ARE IN OHMS, 1/4W, 5%.

SCHEMATIC
HEATER
CIRCUIT
31183-7-2 A

6.2 TIME BASE/ADV-RET SYNCHRONIZER (Dwg. #31209-7-2)

GENERAL

The Time Base/Adv-Ret Synchronizer card performs two functions.

(1) The Time Base section generates a stable, crystal controlled 1 MHz pulse rate. This signal is divided down to 500 kpps and 100 kpps for use in the minor counters and seconds accumulator.

(2) The Advance-Retard Synchronizer section allows synchronizing the clock with an external standard. Various rates are available to facilitate precise adjustment in a minimum time.

TIME BASE

The Time Base section consists of an unheated 1 MHz crystal (Y2) operating in a Colpitts type oscillator (Q3). The resulting 1 MHz signal is applied to a clipper amplifier, Q1. Q1 provides a 5 V p-p 1 MHz pulse rate which is buffered by A6 and applied to gate A9. Functionally, A9 is part of the Adv-Ret circuit and will be explained later. The output of gate A9 is divided by flip-flop A8 to produce both 500 kpps and 100 kpps signals. These signals are buffered for use by other circuits.

ADV-RET SYNCHRONIZER

The Adv-Ret circuit provides a means to add or subtract counts to bring the clock into coincidence with a standard time signal (Such as WWV). Six rates are provided for adding or subtracting count. Of the six, the four slowest rates are selectable with a front panel switch. The full six rates are available when the remote

control is used. Since the operation is identical at all rates, only one will be described. Rate selection is accomplished by grounding the input of the gate for the desired rate.

Refer to the Adv-Ret timing diagram, Figure 1. With the 100 ms/s rate selected, 100 kpps is applied to the clock pulse input of a flip-flop (A4-1). Since both the external J & K inputs are open (High) the output (A4-12) will change from the (Reset) zero state to the one state when the 100 kpps signal goes low. This sets the J input of another flip-flop (A4-7) high, allowing the flip-flop to change state (from zero to one) the first time the 1 MHz clock goes low. Gate A6-11 is used to reset the first flip-flop (A4-12). The output of the gate is held high whenever A4-9 is low. A reset pulse is produced the first time the 1 MHz clock goes high after A4-9 goes high. The reset pulse causes A4-12 to go low which causes A4-9 to go low the nest time the 1 MHz clock goes low. This terminates the reset pulse and completes the cycle. The cycle repeats each time the 100 kpps signal goes low, i.e. every 100 ms. In this way, 100 pulses per second are produced. Each pulse can advance or retard the clock 1 µs.

Selection of either advance or retard is accomplished by a series of gates. Two gates are connected to the input of the divider decade (A8). One (A9-3) is used to inhibit clock pulses for retard, the other (A9-6) is used to add pulses for advance. Gate A6-3 and A7-8 complete the retard selection circuit. A ground on the $\overline{\text{RET}}$ line will enable gate A7-8. This will allow flip-flop A4-9 to control gate A9-3, deleting one pulse each 100 ms.

A flip-flop (A6-8 and A5-8) and gates A7-11 and A5-6 complete the advance circuit. The flip-flop is set by a ground on the $\overline{ADV}$ line and reset every 10 ms by A5-6. When the flip-flop is set (giving a high at A6-8), gate A7-11 is enabled allowing pulses produced at A4-8 to input the divider (A8). Note that the fall time of these pulses occurs at the rise time of the 1 MHz clock out of A9-3. Therefore, an *"extra"* pulse inputs the divider (A8) each 100 ms.

This card additionally provides the non-inverted waveforms for two pulse rates used elsewhere in the unit.

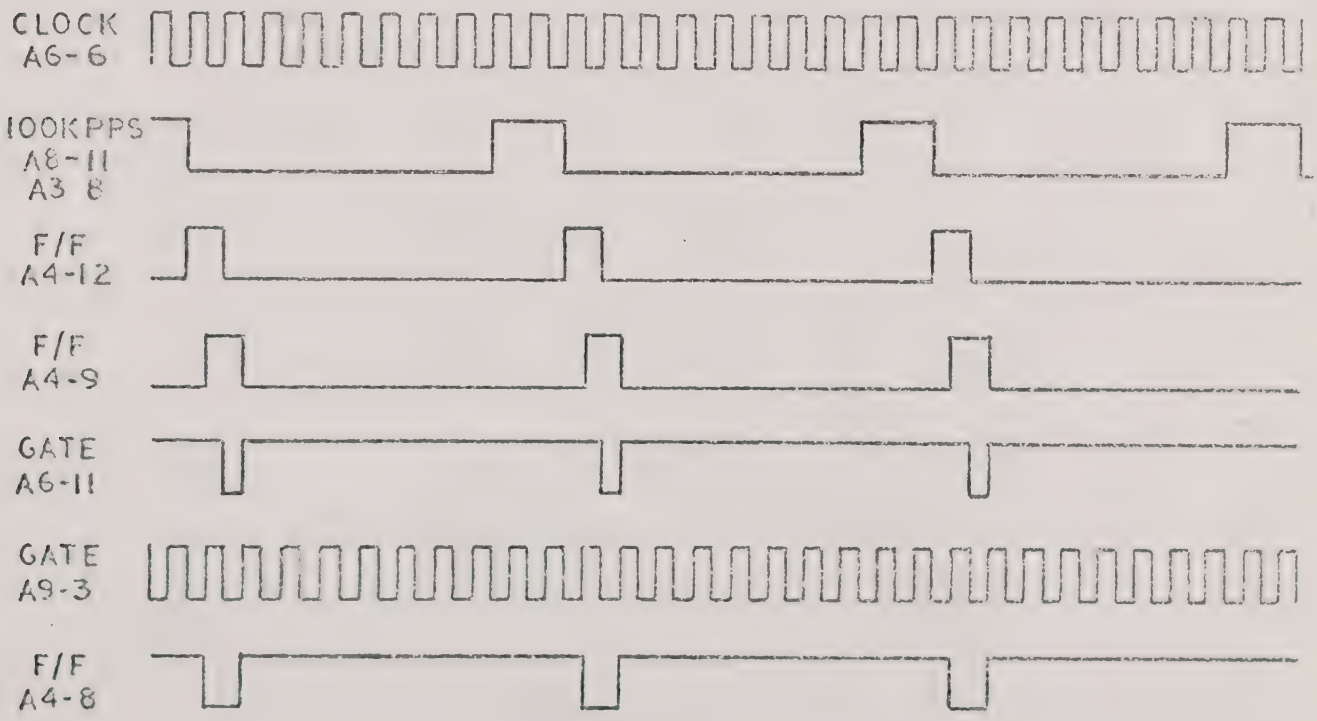


FIGURE 6.1

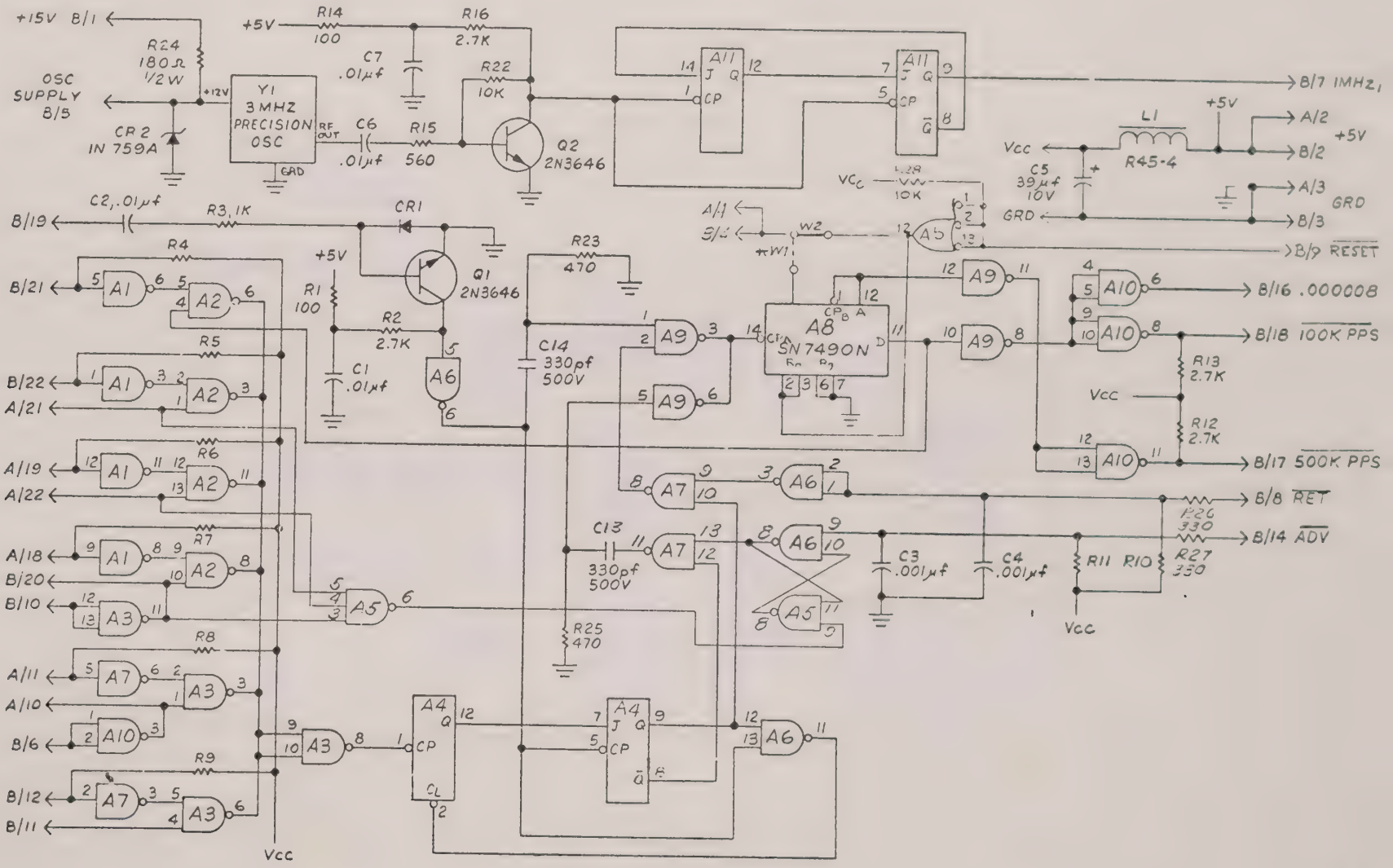
TIMING SEQUENCE
TIME BASE/ADV-RET
SYNCHRONIZER

TIME BASE/ADV-RET SYNCHRONIZER P/L 31209-8-1,2,3
PARTS LIST

Ref.	Description	S-D Part No.
	Assembly	31209-4-2
	Schematic	31209-7-2
CAPACITORS		
C1,2,6,7	Capacitor, 0.01 µf, Disc	C0233
C3,4	Capacitor, 0.001 µf, Disc	C0235
C5,8	Capacitor, 39 µf, 10 V, Tant	C0902
C9	Capacitor, 1-28 PF, var.	C1059 (C0555)
C10	Capacitor, 22 PF, Dip Mica	C0529
C11	Capacitor, 680 PF, Dip Mica	C0638
C12	Capacitor, 3000 PF, Dip Mica	C0759
C13,14	Capacitor, 330 PF, 500 V	C0540
DIODES		
CR1	Diode, 1N4151	CR0150
CR2	Diode, 1N759A	CR0174
INTEGRATED CIRCUITS		
A1,2,3,9,10	Integrated Circuit, L5-846N	19716
A5	Integrated Circuit, SN7401N	19706
A6,7	Integrated Circuit, SN7400N	19705
A8	Integrated Circuit, SN7490N	19711
A4,11	Integrated Circuit, SN7473N	19709
TRANSISTORS		
Q1,2	Transistor, 2N3646	Q0218
Q3	Transistor, 2N2222	Q0116
RESISTORS		
R1	Resistor, 100 Ω, 1/4 W, 5%	R0966
R2,12,13,16	Resistor, 2.7 kΩ, 1/4 W, 5%	R0937
R3	Resistor, 1 kΩ, 1/4 W, 5%	R0765
R4-11	Resistor, 4.7 kΩ, 1/4 W, 5%	R0892
R15	Resistor, 560 Ω, 1/4 W, 5%	R0819
R17	Resistor, 47 Ω, 1/4 W, 5%	R0743
R18	Resistor, 39 kΩ, 1/4 W, 5%	R0748
R19	Resistor, 6.8 kΩ, 1/4 W, 5%	R0696
R14	Resistor, 100 Ω, 1/4 W, 5%	R0966

Ref.	Description	S-D Part No.
R21	Resistor, 220 Ω, 1/4 W, 5%	R0760
R22	Resistor, 10 kΩ , 1/4 W, 5%	R0766
R24	Resistor, 180 Ω, 1/2 W, 5%	R0725
R23,25	Resistor, 470 Ω, 1/4 W, 5%	R1044
R26,27	Resistor, 330, Ω, 1/4 W, 5% CC	R0662
R20	Resistor, 820 Ω, 1/4 W, 5%	R0762
OTHER		
Y1	Oscillator, 3 MHz (JK 013-0160)	Y0045
Y2	Crystal, 1 MHz	Y0019
Y1	Oscillator, 3 MHz	Y0048
H1	Crystal Bracket, AU6AT	H1190
H2	Washer, Nylon #4	H0553
L1	Inductor, R45-4	L0143

31209-7-3



TIME BASE/ADV-RET SCHEMATIC #B31209-7-3F

6.3 TIME BASE/MINOR COUNTERS Dwg. #31210-7-,1,2,3

GENERAL

This card is basically a five decade counter with start/stop gating, reset, and buffered outputs. Logic is also provided to generate square waves at 10 kHz, 1 kHz, and 100 Hz.

START/STOP

The first two decades of the divider are isolated from the remaining three decades to permit presetting propagation delay into the unit when the remote control is used. In this case jumpers W2 and W3 are connected in the alternate configuration, preventing A12 and A10 from resetting when a stop command occurs.

Flip-flop A13 provides a reset signal under two different conditions. A ground on the $\overline{\text{MAN STOP}}$ line will unconditionally set A13 in the stop condition, providing reset. A ground on the $\overline{\text{STOP}}$ line will permit A13 to go to the stop condition the first time the auto stop line goes low. The auto stop line has a negative spike once per second, on time. Removal of the reset signal occurs unconditiona when any of three conditions are satisfied. 1) Ground on the $\overline{\text{RUN}}$ line, 2) Ground on the $\overline{\text{AUTO START}}$ line, or 3) A high on the EXT START line. Transistor Q2 is used as an inverter and a gate for the various start commands. Transistor Q1 is used to remove the input signal to the decade counters during stop to preserve the count in A12 and A10 when using the remote control.

DECADE COUNTERS

Five decade counters are connected to divide by incoming 100 kpps

signal down to 1 pps. Each of the outputs from the decades is buffered and brought out to a pin in an inverted condition. In addition, two outputs (8×10^{-5} and 8×10^{-4}) are double buffered to provide the non-inverted condition. Reset for the last three decades is provided via transistor Q3 when a ground is present on the $\overline{\text{EXT}}$ $\overline{\text{RESET}}$ line.

SQUARE WAVE OUTPUTS

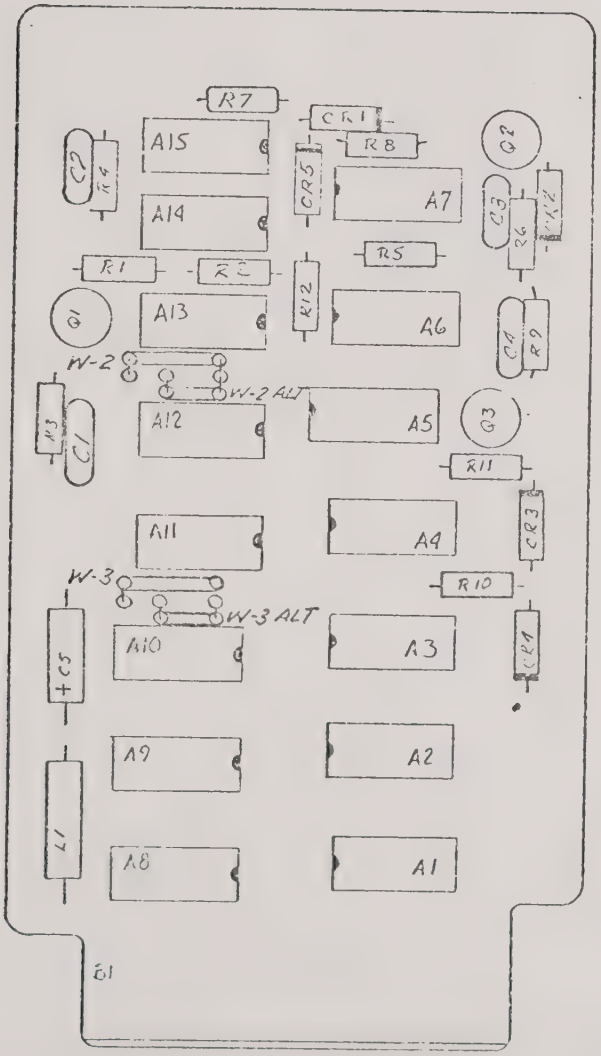
Three square wave signals are provided by this card. Gates A14 decode sufficient lines to give a 10 kHz square wave. Gates A8 yield 1 kHz and gates A7, 100 Hz.

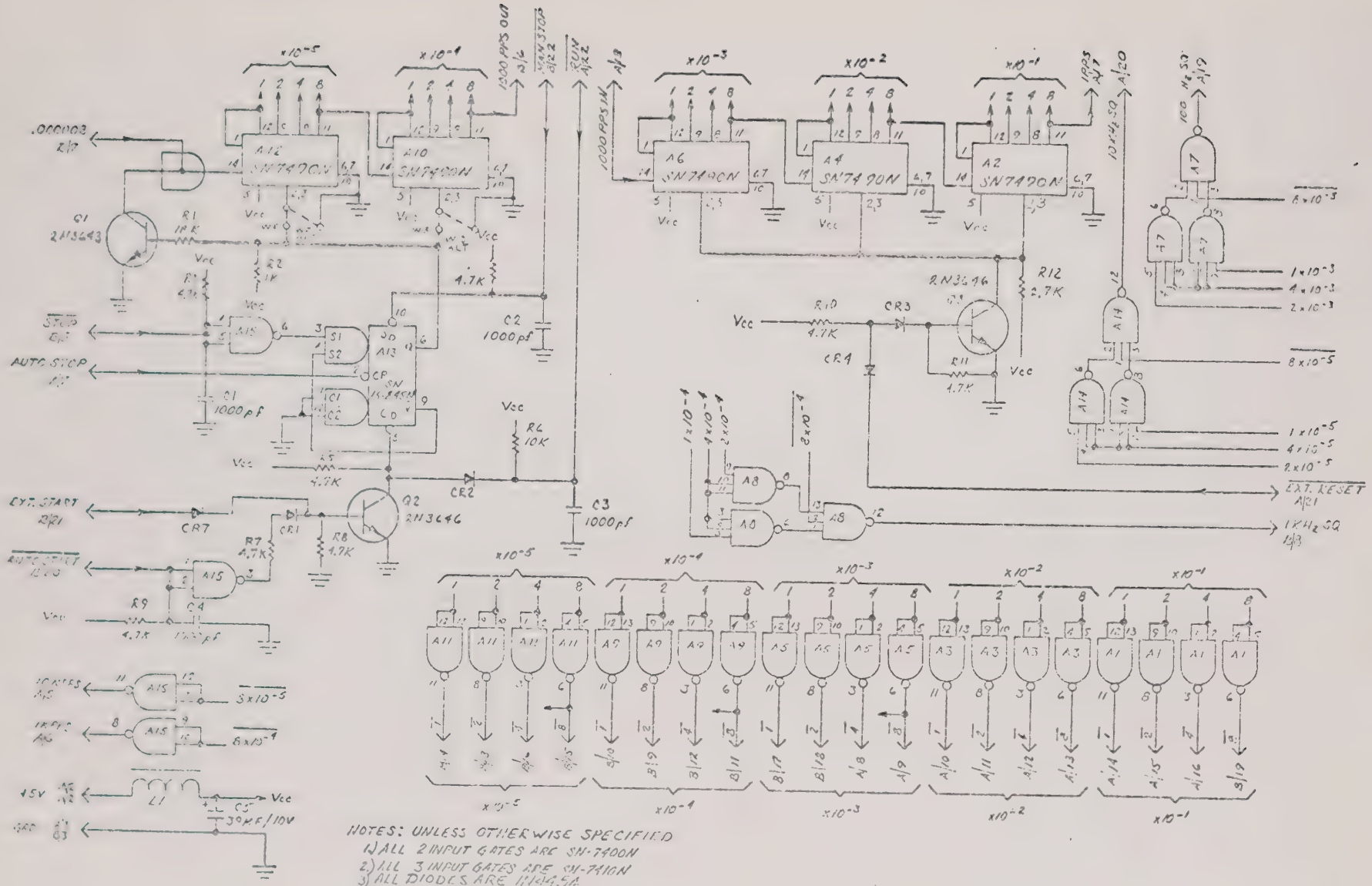
PARTS LIST

TIME BASE/MINOR COUNTERS P/L 31210-7-1,2,3,4 or

Ref.	Description	S-D Part No.
	Assembly	31210-4-1
	Schematic	31210-7-1
C1-4	Capacitor, 1000 pf	C0543
C5	Capacitor, 39 µf, 10 V	C0902
CR1-5	Diode, 1N4151	CR0150
A1, 3, 5, 9, 11	Integrated Circuit, SN7400N	19705
A2, 4, 6, 10, 12	Integrated Circuit, SN7490N	19711
A7, 8, 14	Integrated Circuit, SN7410N	19706
A13	Integrated Circuit, SN15-845N	19715
Q1	Transistor, 2N3643	Q0179
Q2-3	Transistor, 2N3646	Q0218
R1	Resistor, CC, 18 kΩ, 1/4 W, 5%	R0785
R2	Resistor, 1 kΩ, 1/4 W, 5%, CC	R0765
R3-5, 7-11	Resistor, 4.7 kΩ, 1/4 W, 5%, CC	R0892
R6	Resistor, 10 kΩ, 1/4 W, 5%, CC	R0766
R12	Resistor, 2.7 kΩ, 1/4 W, 5%, CC	R0937
L1	Inductor, R45-4	L0143

ASSEMBLY
TIME BASE/MINOR COUNTER
31210-4-1 G





NOTES: UNLESS OTHERWISE SPECIFIED
1) ALL 2 INPUT GATES ARE SN-7400N
2) ALL 3 INPUT GATES ARE SN-7410N
3) ALL DIODES ARE 1N4454A
4) VCC IS CONNECTED TO PIN 14 ON A1, A3, A5, A7, A8, A9, A11, A13, A15
5) GRD IS CONNECTED TO PIN 7 ON A1, A3, A5, A7, A8, A9, A11, A13, A15

SCHEMATIC
TIME BASE/
MINOR
COUNTERS
31210-7-1 G

6.4 SWITCHABLE IRIG DC CODE GENERATOR Dwg. #31044-7-5

General

This card fully assembled, permits generation of any one of IRIG A, B, C, or E codes. Code selection may be remotely controlled. A dc level shift output is produced. By leaving out certain IC circuits, this card is modified to produce only the IRIG B, hours, minutes, and seconds format.

Divider Circuits

Refer to timing diagrams, Figures 6.2 & 6.3 for this and all following sections. Divider A11 is a divide by two then by five counter which divides down the "Z RATE" and provides decoded outputs for the code generating gates. Divider A12 is a divide by five then by two counter which takes the output of A11, divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider A15 is a divide by two then by six counter. Its principal function is to control the secondary scan gate A10. The division by twelve is used only for IRIG C, the divider being reset at the count of ten for the other codes. This early reset is shown on the timing diagram as A19-6. The reset pulse is quite short and therefore has been widened for clairty. The area between the dotted lines on sheet two is simply eliminated when the divider resets at ten. Reset at ten is established by gate A19-6. A one shot, A19-8 and A19-12 performs code frame reset. An external reset signal may be used for code frame reset when W1 is installed, or this card will supply a reset pulse to synchronize the associated accumulator when W2 is installed.

Scan Gates

Creation of serial ones is accomplished by a two stage switching network and a series of gates. Switches A1-A5 are basically single pole (pin 8 is the output) 8 position switches. The switching is controlled by BCD information on pins 1, 2, and 13. Since all five switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus the need for switch A10. This switch, controlled from the BCD outputs of divider A15, selects the proper time interval for serializing each switch output. The series of gates connected to A1 and A2 outputs further control those switches which have output that should not be present in certain codes. Tenths of seconds are added only in IRIG A unit seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates A9-6, A13-8, and A18-8 are used to inhibit the presence of serial ones at certain times when no serial ones should be present. This prevents the spurious "ones" coming from the switches from appearing in the output code.

Code Generating Gates

These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the "Z RATE" on pin A13. A 2 length is a ZERO, a 5 is a ONE, and an 8 is an INDEX MARKER. The INDEX MARKERS are generated by gating the output of divider A12. Gate A13 adds information from the output of divider A11 to create the "8" width. Gates A9-3 and A9-11 allow an extra pulse from gates A8-3 and A13-6 to give the "double mark" at the start of the frame. Gate A17-6 provides the marker at each tenth frame interval.

Gate A18-3 supplies a pulse of "Z" width at the start of each bit interval. If a MARKER or a ONE is not present then the output code will be high for only the "Z" width. Gate A16-3 supplies the "5" width pulse. This is AND gated with the $\overline{\text{SERIAL ONES}}$ from A18-8 by gate A16-11. The presence of a ONE will cause the "5" width to appear in the output code, masking the "2" width which is always present. Gates A16-8 and A18-6 are used to combine the various widths to produce the outputs code.

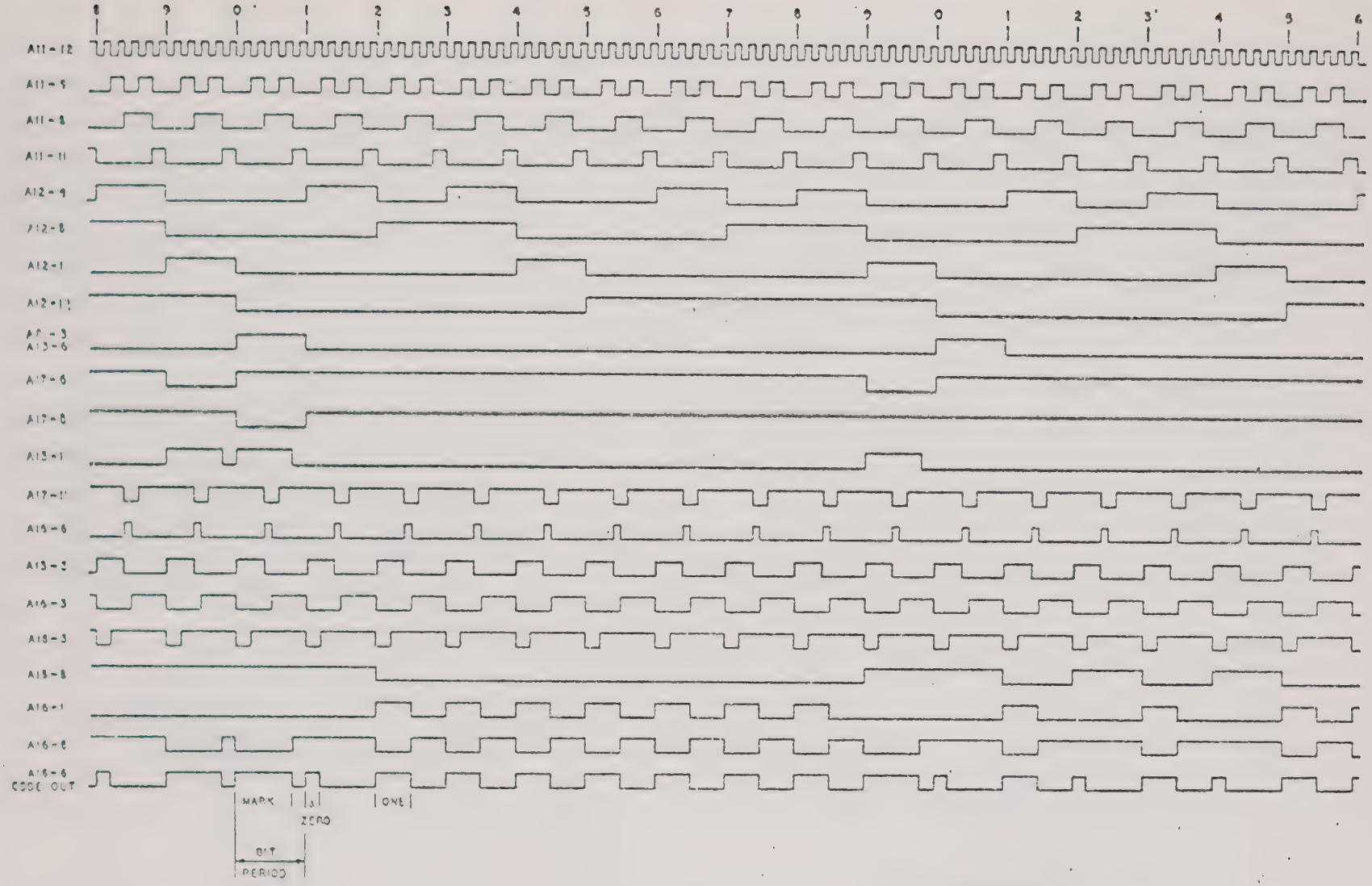
Spur Counter

Divider A14, when included on this card is used to provide an additional divide by five circuit. Its primary use is in generating the IRIG C code Z rate from the 100 pps rate available elsewhere in the unit. It is synchronized with the common frame reset line.

PARTS LIST

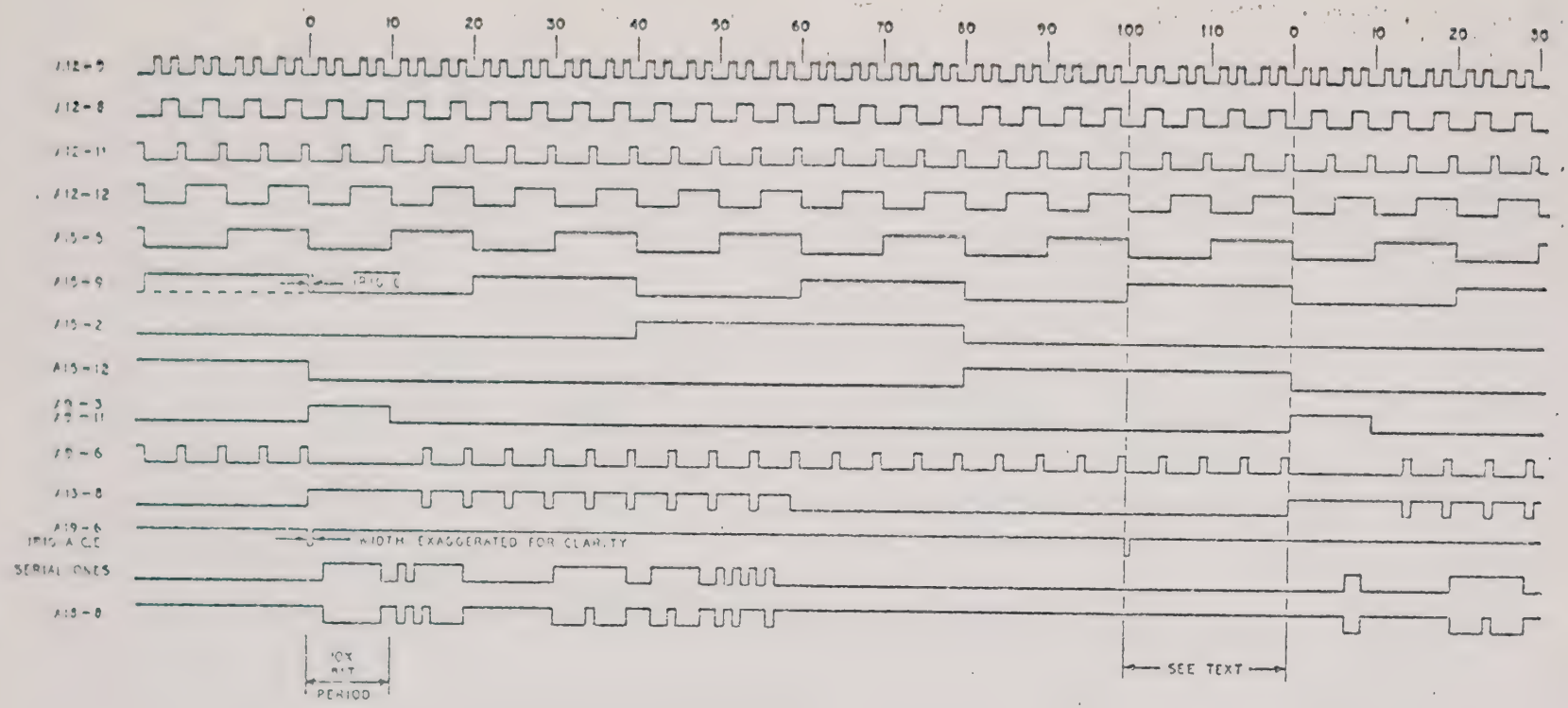
IRIG SWITCHABLE DC CODE GENERATOR P/L 31044-8

Ref.	Description	S-D Part No.
	Assembly	31044-4-5
	Schematic	31044-7-5
A1,2,3,4,5, 10	Integrated Circuit, DM8210	25746
A6,17,18	Integrated Circuit, MC846P	19716
A7	Integrated Circuit, MC836P	25704
A8,9,13,16	Integrated Circuit, MC1810P	25735
A11	Integrated Circuit, SN7090N	25732
A12	Integrated Circuit, SN7490N	19711
A14	Integrated Circuit, SN8280A	25722
A15	Integrated Circuit, C2125A	25723
A19	Integrated Circuit, SN7410N	19706
C1	Capacitor, 39 µf, 10 V	C0902
C2	Capacitor, 0.01 µf	C0556
R1	Resistor 390 Ω, 1/4 W, 5%	R0880
L1	Inductor, R45-4	L0143
	Extractor	H1743



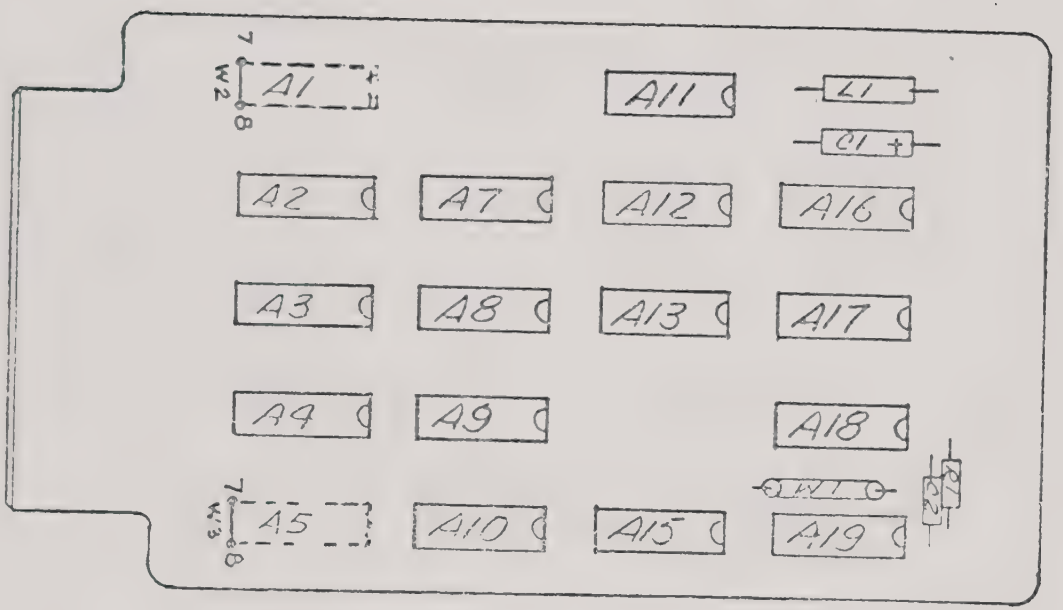
NOTE
CODE SHOWN IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

FIGURE 6.2
TIMING DIAGRAM
SWITCHABLE
IRIG DC CODE
31581-7-1 Sheet 1

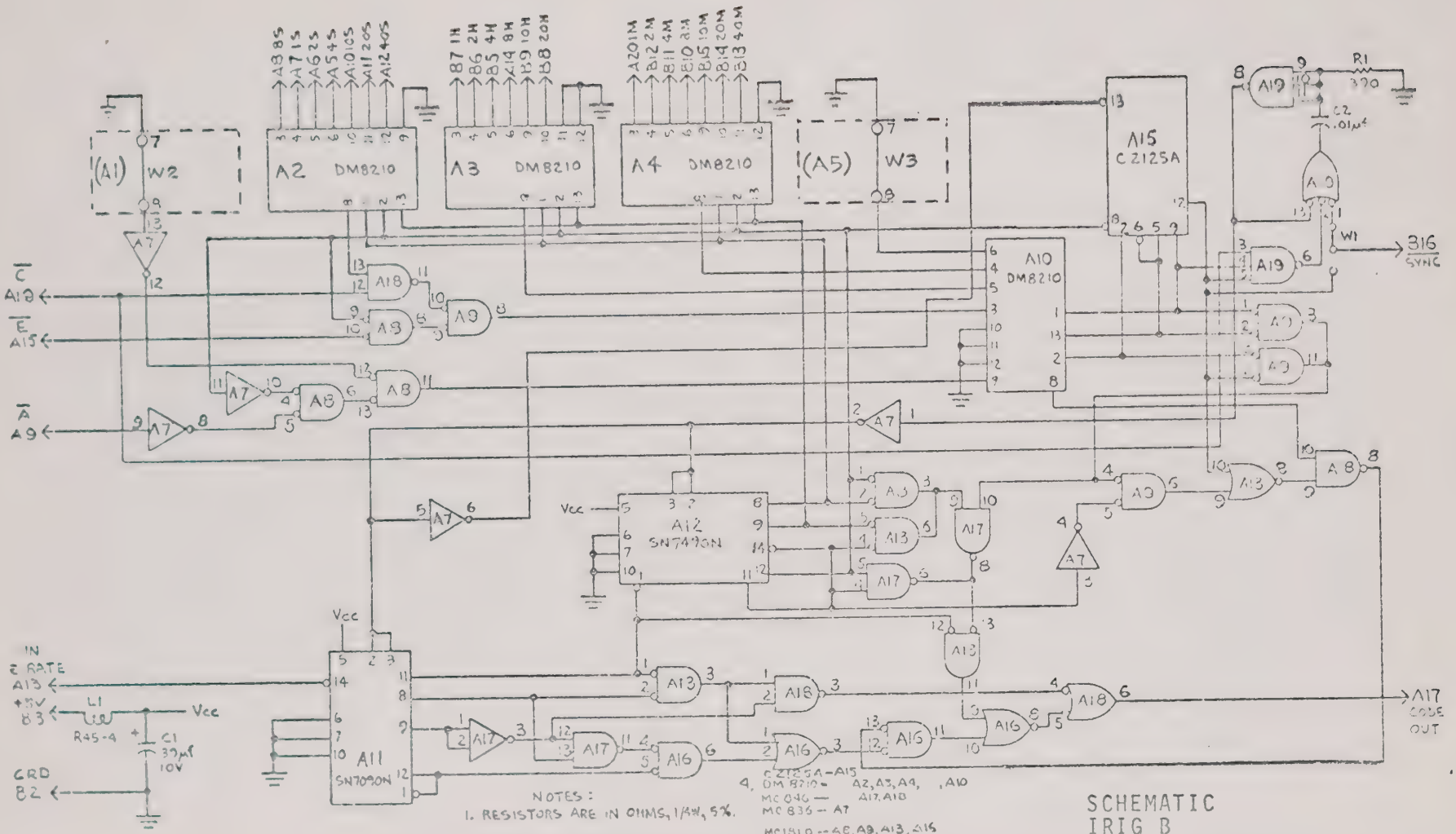


NOTE:
CODE SHOWN (SERIAL ONES & A18-8) IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

FIGURE 6.3
TIMING DIAGRAM
SWITCHABLE
IRIG DC CODE
31581-7-1 Sheet 2



ASSEMBLY
IRIG SWITCHABLE
DC CODE GENERATOR
PC BOARD
31044-4-5


A2 DM8210
A3 DM8210
A4 DM8210
(A1) W2
(A5) W3
A15 CZ125A
A10 DM8210
A12 SN7490N
A11 SN7090N
R1 330
C2 .01μF
W1
316 SYNC
A17 CODE OUT
IN 2 RATE A13
+5V B3
GRD B2
L1
R45-4
C1 33μF 10V
Vcc
NOTES:
1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 7 OF ALL IC'S. IS CONN. TO GRD.
" 14 " " " " " " Vcc
4, DM8210 — A2, A3, A4, , A10
MC040 — A17, A18
MC836 — A7
MC1810 — A6, A8, A13, A15
SN7490 — A12
SN7410 — A16
SN7050 — A11
CZ125A — A15
SCHEMATIC
IRIG B
DC CODE GENERATOR
31044-7-5 A

6.5 TIME-OF-DAY ACCUMULATOR Dwg. #31501-7-2

General

This card contains circuitry to totalize the 1-pps signal and produce parallel BCD outputs of hours, minutes, and seconds. Additional circuitry controls reset an fast update for serial preset. The card in 21502-7-2 configuration is assembled to produce a 24 hour recycle.

Fast Update Circuit

When the REMOTE CONTROL unit is used with the unit, provision is made for serially updating all the accumulators at a 100 kHz rate. Switches on the remote control unit set the time to be preset and a signal is sent by the remote to indicate when the accumulators in coincidence with the preset switches, causing the update to stop. Flip-flop A12 provides a fast update enable signal under proper conditions. This signal allows a 100 kpps signal to input the accumulators in place of the normal 1 pps. Gates A14-3 and A14-6 perform the selection.

A number of conditions must be present to allow the fast update to preset the accumulators. The $\overline{\text{PRESET TIME}}$ line must be grounded. This signal is open (High) when either "START" or "RUN" modes are selected. With the $\overline{\text{PRESET TIME}}$ line open, transistor Q1 will be turned on, holding A17 in a clear condition and preventing fast update. Also, even with the $\overline{\text{PRESET TIME}}$ line at ground, a reset command will turn Q1 on via the wired OR. Assuming Q1 is off,

fast update is initiated by a ground on the $\overline{\text{TIME}}$ $\overline{\text{PRESET}}$ line (Pin B/19). Note that a preset time signal (This is $\overline{\text{PRESET}}$ $\overline{\text{TIME}}$ inverted by A18-6) is used to hold off the $\overline{\text{TIME}}$ $\overline{\text{PRESET}}$ at the same time that A17 is held in a clear condition. A one shot (A18-3 and A18-11) pulses the steering gates of A17 to start the update. The preset time signal is again used at this point. When the accumulators reach the same number that was preset, a ground on the $\overline{\text{COINC.}}$ $\overline{\text{TIME}}$ line from the remote control unit is inverted by A14-11 and shuts off the fast update. Note that the $\overline{\text{PRESET}}$ $\overline{\text{TIME}}$ signal is used to disable the 1 pps input except in Start and Run modes via R20, C11, and CR1.

Reset Circuit

Reset for all the accumulators is initiated by a ground on Pin B/13, $\overline{\text{TIME}}$ $\overline{\text{RESET}}$. Again, the preset time signal is used to prevent reset via the $\overline{\text{TIME}}$ $\overline{\text{RESET}}$ line when in start or run modes. An $\overline{\text{EXT}}$ $\overline{\text{RESET}}$ line (Pin B/20) is available which will always supply a reset command. A one shot A15-12 and A15-6, plus inverter A15-8 provides a 250 μs pulse for reset.

Accumulator Circuit (seconds)

The gated 1 pps signal is fed to two dividers, A12 and A16. A12 divides by ten, A16 by six. BCD is provided from each divider as well as a 1 ppm pulse for the hours accumulator. Each output is buffered with the non-inverted outputs brought out.

Accumulator Circuit (minutes)

Two dividers, A2 and A4, are used to first divide the 1 ppm signal by 10 and then by 6, producing a 1pph signal. BCD signals are buffered with the non-inverted outputs brought out. Reset is provided for each divider.

Accumulator Circuit (hours)

Two decade counters A6 and A8 divide the 1 pph input signal down until recycle occurs at either 24 or 48 or 99 hours. An output signal for a days counter may be taken from either a "20" or "40" or "80" output, depending on the recycle time selected. The BCD outputs are buffered with the non-inverted outputs brought out.

Recycle Circuit

The hours accumulator may be reset to zero either by the external reset signal on Pin A/8, via gate A10 and one shot A9, or by one of two AND gates. One of these gates, when C16 is connected, will provide a pulse to one shot A9 when the counter reaches 24 hours, resetting the counter to zero. The other gate, via C17, will perform reset at 48 hours. With neither capacitor in the circuit reset will occur at 99 (100 HRS).

Accumulator Circuit (minutes)

Two dividers, A2 and A4, are used to first divide the 1 ppm signal by 10 and then by 6, producing a 1pph signal. BCD signals are buffered with the non-inverted outputs brought out. Reset is provided for each divider.

Accumulator Circuit (hours)

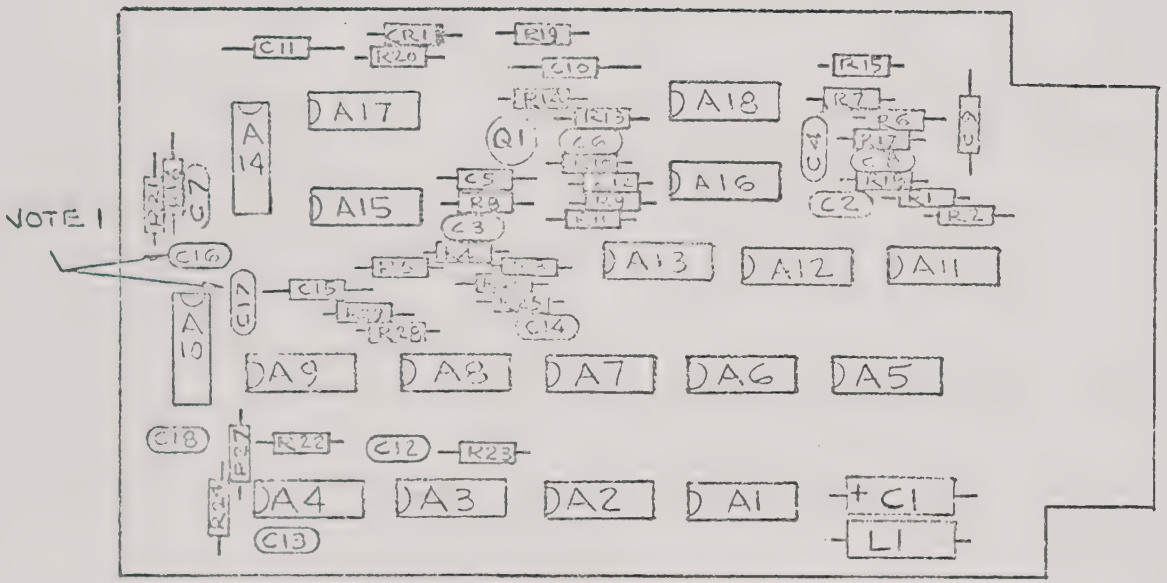
Two decade counters A6 and A8 divide the 1 pph input signal down until recycle occurs at either 24 or 48 or 99 hours. An output signal for a days counter may be taken from either a "20" or "40" or "80" output, depending on the recycle time selected. The BCD outputs are buffered with the non-inverted outputs brought out.

Recycle Circuit

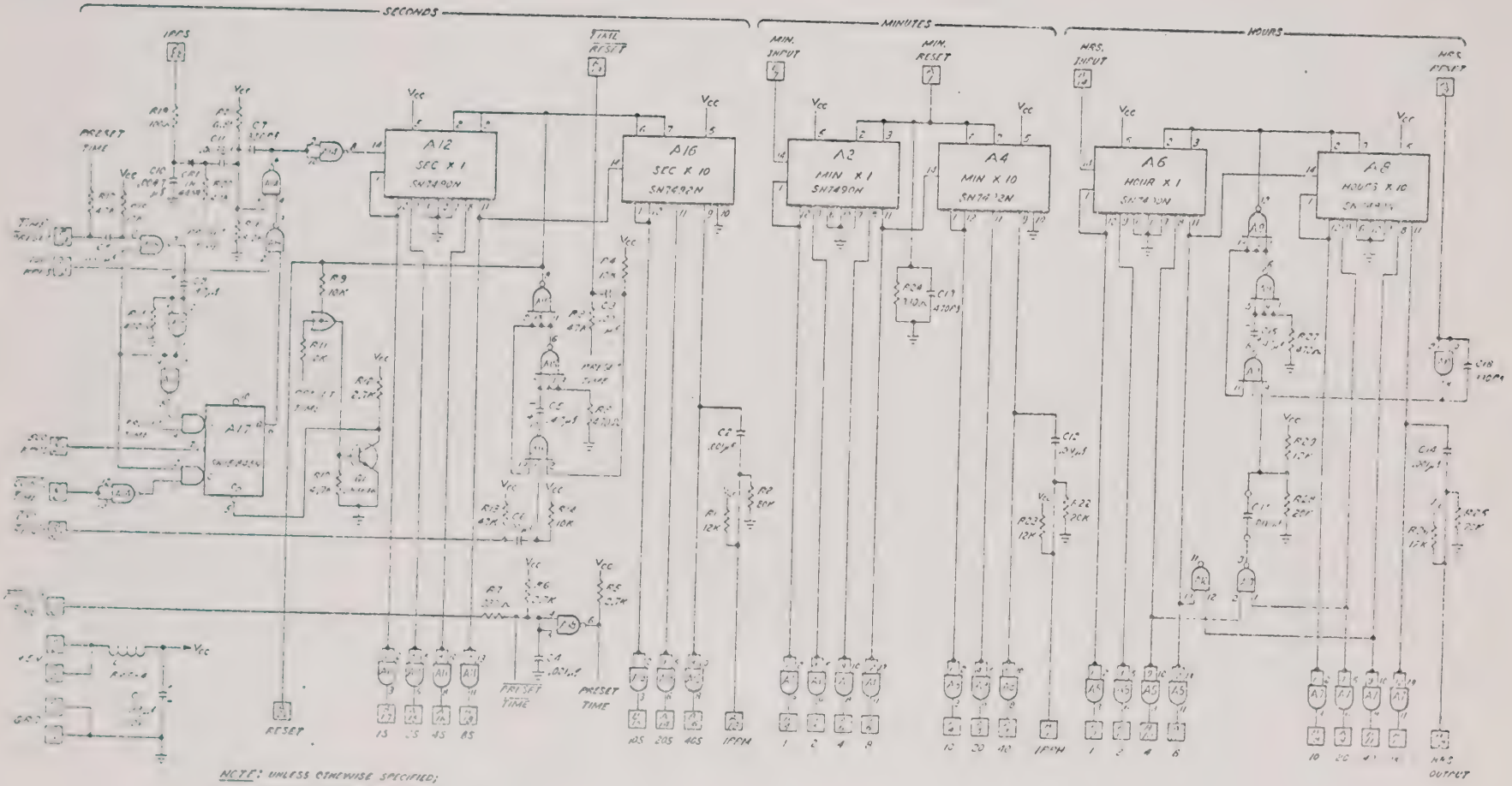
The hours accumulator may be reset to zero either by the external reset signal on Pin A/8, via gate A10 and one shot A9, or by one of two AND gates. One of these gates, when C16 is connected, will provide a pulse to one shot A9 when the counter reaches 24 hours, resetting the counter to zero. The other gate, via C17, will perform reset at 48 hours. With neither capacitor in the circuit reset will occur at 99 (100 HRS).

PART LIST

Ref.	Description	S-D Part No.
	Assembly	31501-4-1
	Schematic	31501-7-1
A1,3,5,7, 11,13	IC MC1806P	25733
A2,6,8,12	IC SN7490	19711
A4,16	IC SN7492N	23442
A9,15	IC SN7410N	19706
A10,14,18	IC SN7400N	19705
A17	IC SN15-845N	19715
C1	Capacitor 39 µf 10 V Tant	C0902
C2,3,4,6,8 12,14,16,17	Capacitor 0.001 µf DM15	C0543
C5,9,15	Capacitor 0.47 µf Tant	C0733
C7,18	Capacitor 330 pf DM15	C0540
C10	Capacitor 0.0047 µf SPR-192P	C0698
C11	Capacitor 0.0033 µf SPR-192P	C0774
C13	Capacitor 470 pf DM15	C1078
CR1	Diode IN4454	CR0150
R1,23,26,29	Resistor 12 kΩ 1/4 W 5% CC	R0759
R2,22,25,28	Resistor 20 kΩ 1/4 W 5% CC	R0964
R3,13,17,20	Resistor 47 kΩ 1/4 W 5% CC	R0777
R4,9,11,14, 18	Resistor 10 kΩ 1/4 W 5% CC	R0766
R5,6,12	Resistor 2.7 kΩ 1/4 W 5% CC	R0937
R7,24	Resistor 330 Ω 1/4 W 5% CC	R0662
R10	Resistor 4.7 kΩ 1/4 W 5% CC	R0892
R16	Resistor 8.2 kΩ 1/4 W 5% CC	R0883
R19	Resistor 100 Ω 1/4 W 5% CC	R0966
R21	Resistor 6.8 kΩ 1/4 W 5% CC	R0696
R8,15,27	Resistor 470 Ω 1/4 W 5% CC	R1044
Q1	Transistor 2N3646	Q0218
	Inductor R45-4	L0143
	Extractor	H1743



ASSEMBLY
TIME-OF-DAY
ACCUMULATOR
31501-4-1



NOTE: UNLESS OTHERWISE SPECIFIED;

1. RESISTORS: IN OHMS, ¼W, 5%, C.C.
2. ALL I.C.'S PIN 7 IS CONNECTED TO GRD.
3. ALL " " 14 " " " " Vcc.
4. MICROP - A1, A3, A5, A7, A11 & A13.
   SN7413N - A9 & A15.
   SN7400N - A10, A14 & A18.

SCHEMATIC
TIME-OF-DAY
ACCUMULATOR
(24 HR. RECYCLE)
31501-7-2

6.6 DUAL SHAPER MODULATOR Dwg. #31216-7-4

General

This card is used to provide the modulated code at a 1 kHz rate. Buffers for the dc code are provided as are auxiliary circuit for use in processing various external signals.

1 kHz Shaper Circuit

The modulated code is produced by shaping the 1 kHz square wave converting it to a sine wave and varying the amplitude of the sine wave with the dc code signal.

The 1 kHz square wave at pin B/13 is inverted by gate A3-8, integrated by R8 and C4 and applied to the base of constant current generator Q4. Q3 is an amplifier with C4 providing capacitive feedback. This makes the amplifier appear to have an inductive reactance. Capacitor C5 gives the circuit the electrical properties of a tuned circuit, with R13 providing fine frequency adjustment. R12 is factory selected to allow R4 to cover the desired adjustment range.

The modulator consists of a resistive network and a field effect transistor, used as a switch. Resistors R18, R21, and R23, and potentiometer R22 set the "MARK TO SPACE RATIO". The FET, Q6 switches from a virtual open circuit to a low impedance at a rate determined by the dc code signal on its gate. This causes the resistance ratio to change, changing the voltage which is fed to the output amplifier.

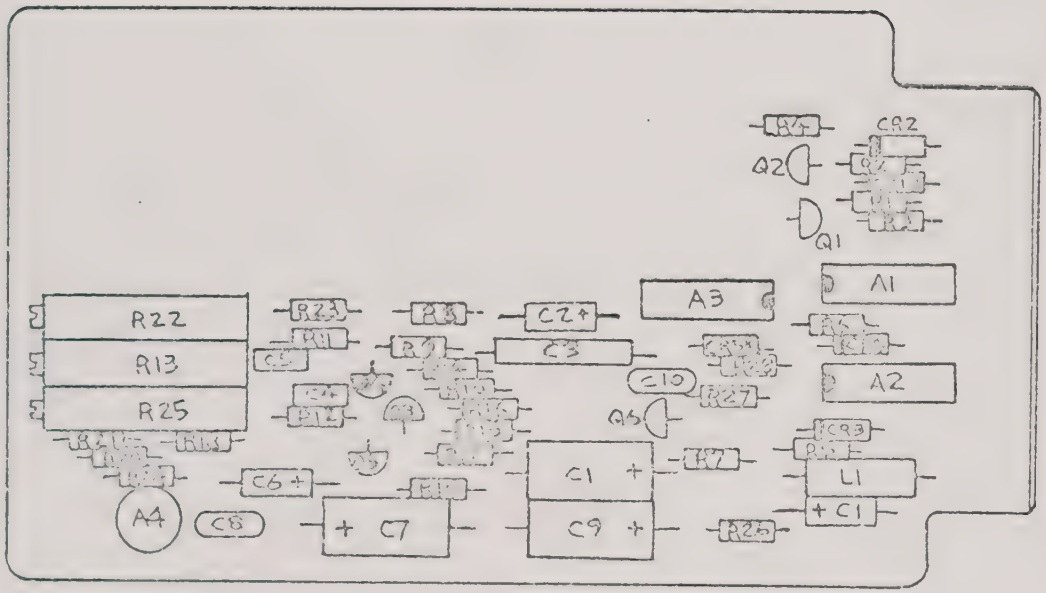
The output amplifier, A4, provides a low impedance source and allows adjusting (with R25) the peak output voltage.

PARTS LIST

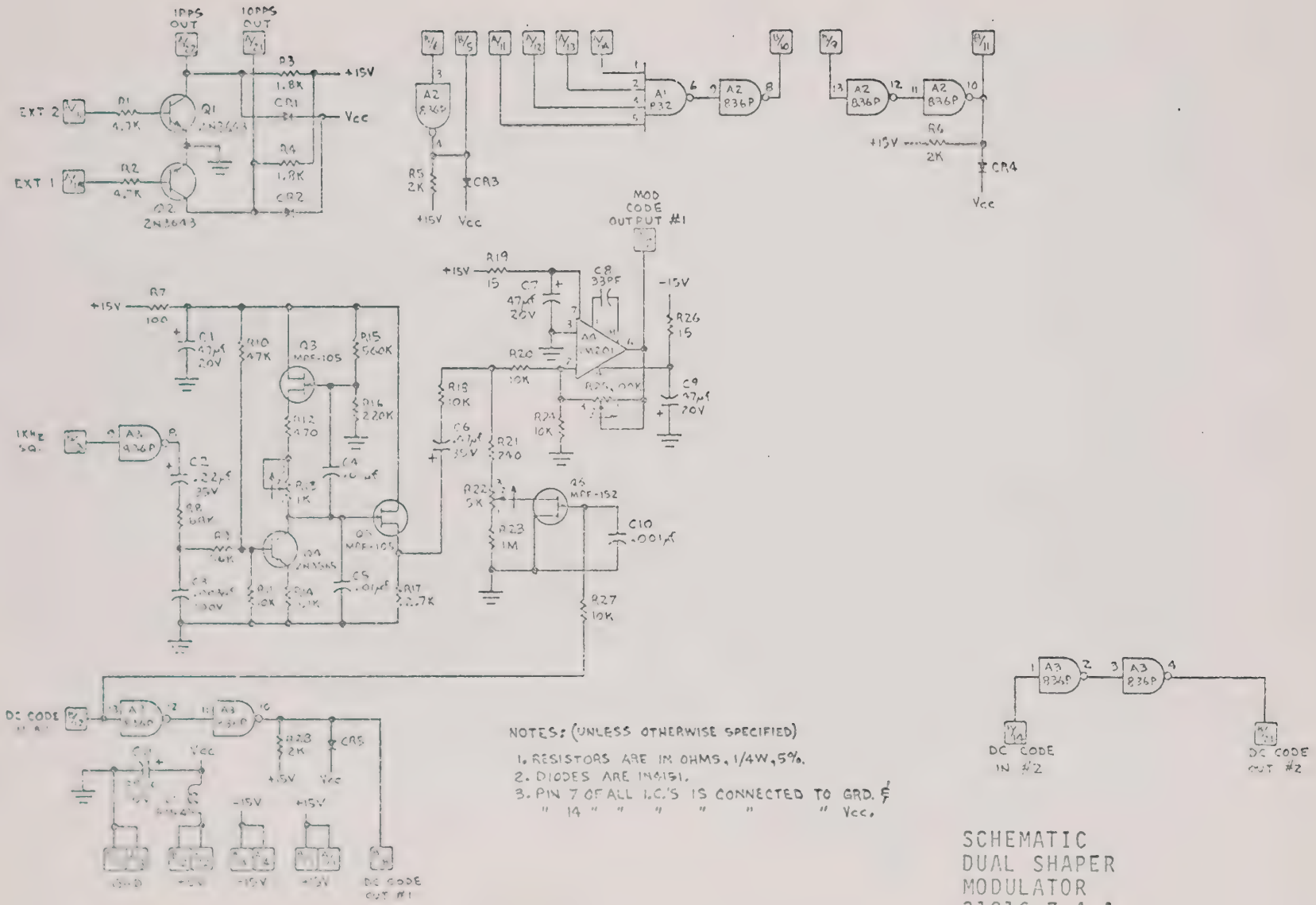
Ref.	Description	S-D Part No.
	Assembly	31216-4-4
	Schematic	31216-7-4
A1	Integrated Circuit, SN15-832N	19713
A2,3	Integrated Circuit, MC836P	25704
A4	Integrated Circuit, LM301A	25745
C1,7,9	Capacitor, 47 µf, 20 V, Tant	C0924
C2	Capacitor, 0.22 µf, 35 V, Tant	C0354
C3	Capacitor, 0.0033 µf, 300 V, Mylar	C0999
C4,5	Capacitor, 0.01 µf, 50 V, Mylar	C0705
C6	Capacitor, 0.47 µf, 35 V, Tant	C0733
C8	Capacitor, 33 pf, DM15	C0531
C10	Capacitor, 0.001 µf, DM15	C0543
C11	Capacitor, 39 µf, 10 V, Tant	C0902
CR1-CR5	Diode, 1N4151	CR0150
R1,2	Resistor, 4.7 kΩ, 1/4 W, 5%	R0892
R3,4	Resistor, 1.8 kΩ, 1/4 W, 5%	R0959
R5,6,8	Resistor, 2 kΩ, 1/4 W, 5%	R0734
R7	Resistor, 100 Ω, 1/4 W, 5%	R0966
R8	Resistor, 68 kΩ, 1/4 W, 5%	R0891
R9	Resistor, 56 kΩ, 1/4 W, 5%	R1235
R10	Resistor, 47 kΩ, 1/4 W, 5%	R0777
R11,18,20 24,27	Resistor, 10 kΩ, 1/4 W, 5%	R0766

PARTS LIST (continued)

Ref.	Description	S-D Part No.
R12	Resistor, 470 Ω, 1/4 W, 5%	R1044
R13	Potentiometer, 1 kΩ, Bourns 224-P	R2248
R14	Resistor, 5.1 kΩ, 1/4 W, 5%	R0693
R15	Resistor, 560 kΩ, 1/4 W, 5%	R1321
R16	Resistor, 220 kΩ, 1/4 W, 5%	R0967
R17	Resistor, 2.7 kΩ, 1/4 W, 5%	R0937
R19,26	Resistor, 15 Ω, 1/4 W, 5%	R1607
R21	Resistor, 240 Ω, 1/4 W, 5%	R0835
R22	Potentiometer, 5 kΩ, Bourns 224-P	R2174
R23	Resistor, 1 MΩ, 1/4 W, 5%	R0962
R25	Potentiometer, 100 kΩ, Bourns 224-P	R2191
Q1,2	Transistor, 2N3643	Q0179
Q3,Q5	Transistor, MPF-105	Q0264
Q4	Transistor, 2N3565	Q0237
Q6	Transistor, MPF-152	Q0263
	Inductor, R45-4	L143
	Extractor	H1743



ASSEMBLY
DUAL SHAPER
MODULATOR
31216-4-4 A



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. DIODES ARE IN4151.
3. PIN 7 OF ALL I.C.'S IS CONNECTED TO GRD. &
   " 14 " " " " " " " Vcc.

SCHEMATIC
DUAL SHAPER
MODULATOR
31216-7-4 A

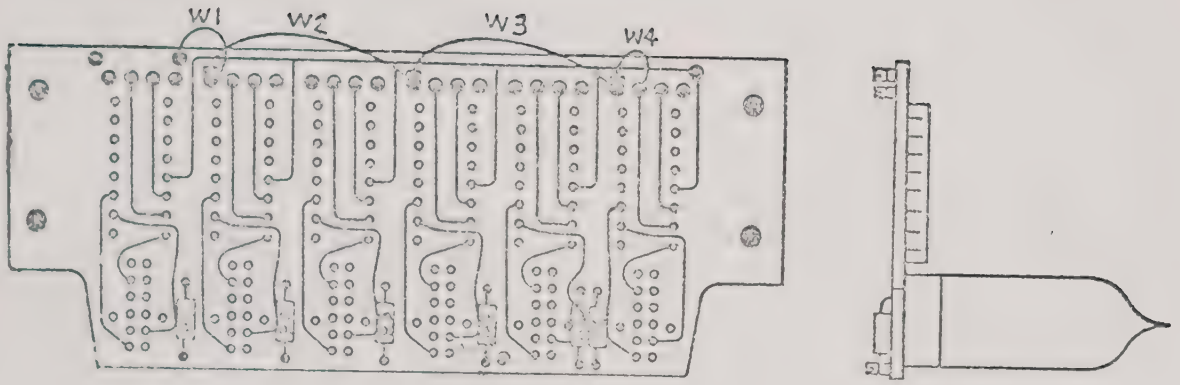
6.7 FRONT PANEL READOUT Dwg.#31195-7-2

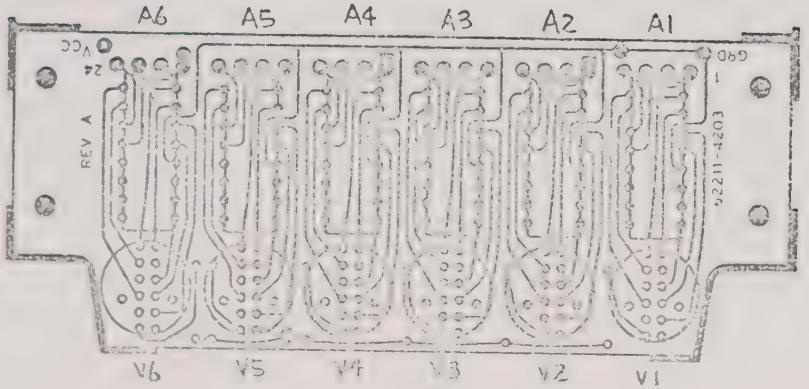
GENERAL

The Readout board has provision for six BCD to decimal converters and six sockets for the indicator tubes. The BCD lines from the accumulators input the converters and +200 V is supplied to run the indicators.

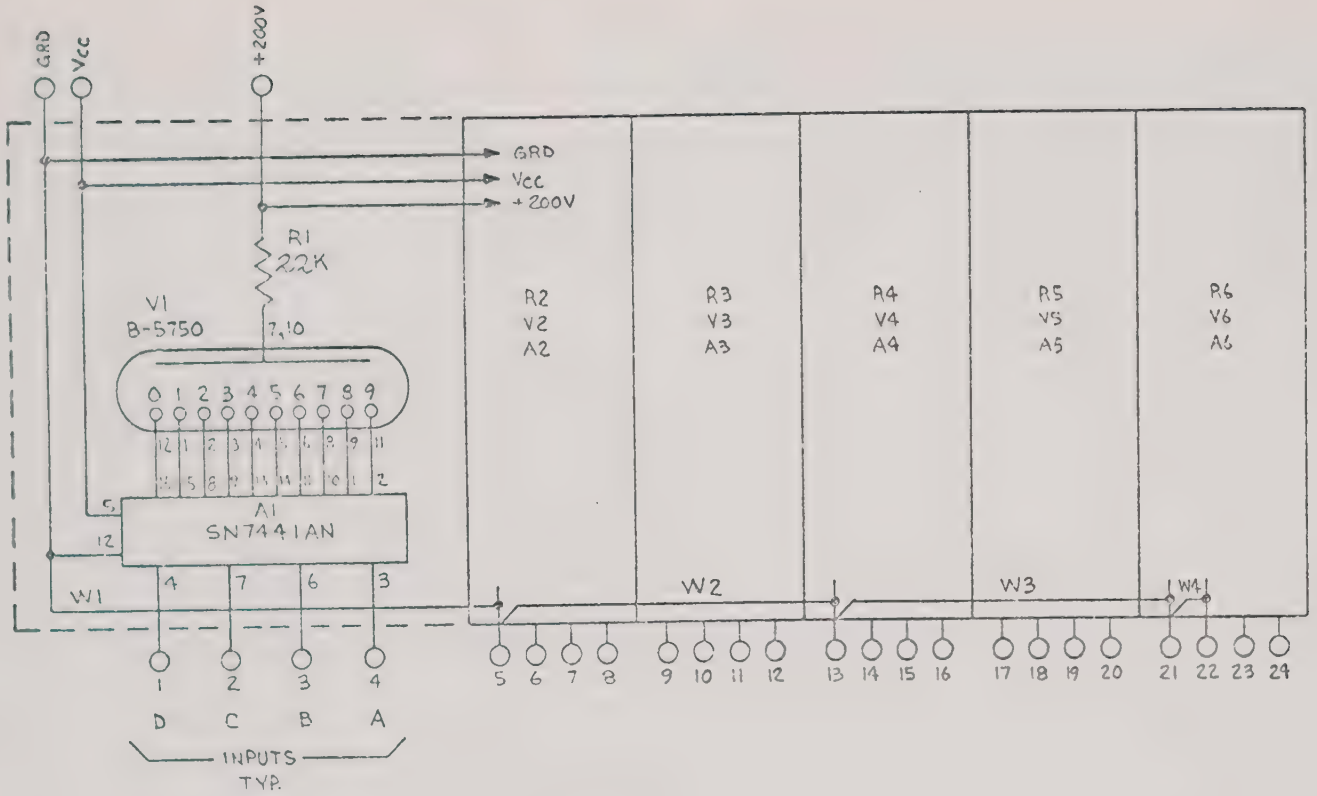
PARTS LIST

Ref.	Description	S-D Part No.
	Assembly	31195-4-1
	Schematic	31195-7-2
A1-6	IC, SN7441AN	19707
R1-6	Resistor, 22 k Ω, 1/4 W, 5%	R0768
V1-6	Tube, Burroughs B-5750	V0123
W1-4	Jumper Wire Insulated	
	Terminal, USECO 2000B	E0100



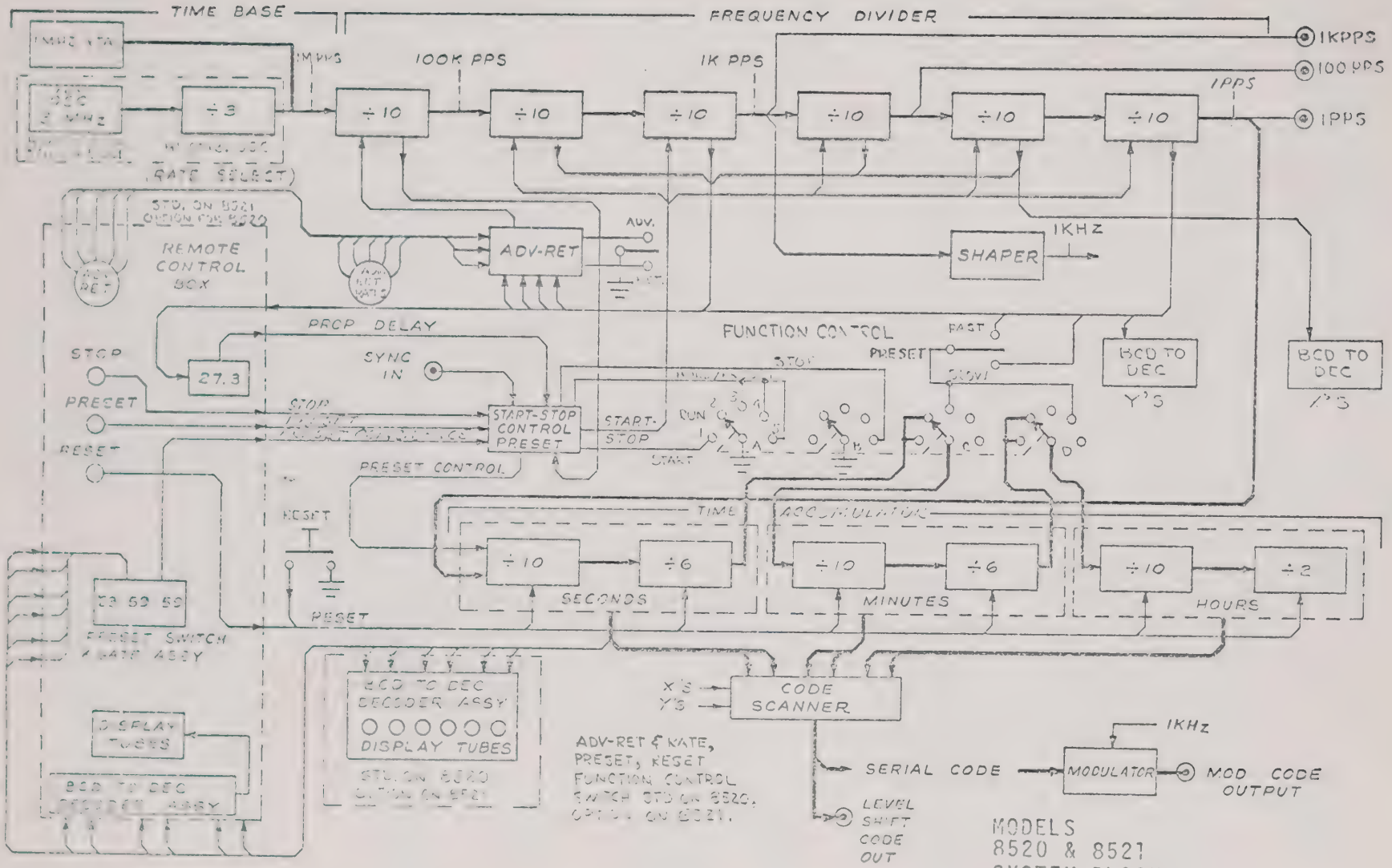


ASSEMBLY
READOUT BOARD
31195-4-2



NOTE:
1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. CIRCUIT SHOWN IS TYPICAL (6) PLACES.
3. W1-W4 ARE ON G2 ONLY.

SCHEMATIC
READOUT
31195-7-2 A

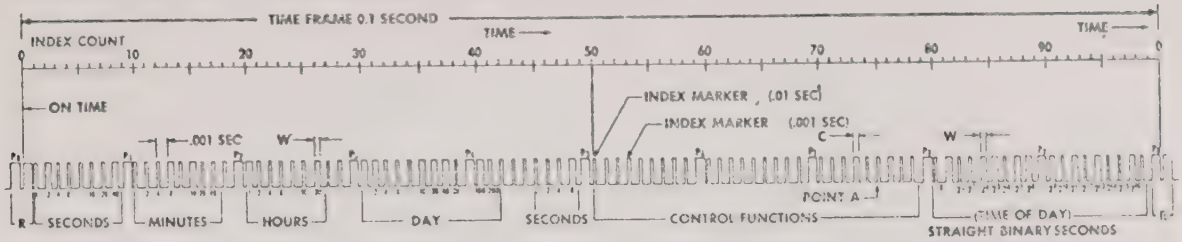


MODELS
8520 & 8521
SYSTEM BLOCK
DIAGRAM
21792-0-1

IRIG TIME CODE FORMATS

FORMAT A

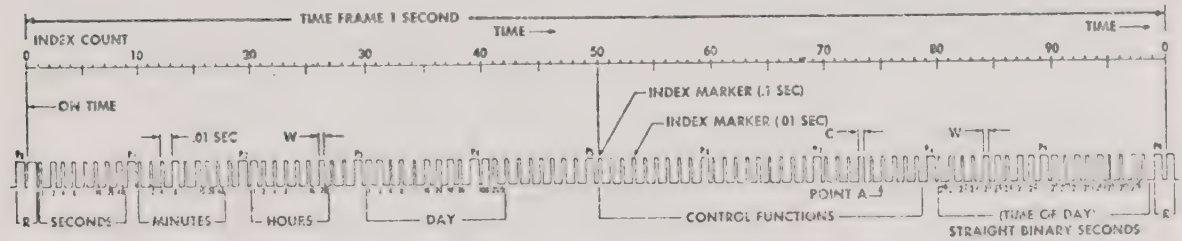
1000-PPS, 34-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A = 21:18:42 + .8 + .07 + .005 21 HR.18 MIN. 42.875 SEC. ON DAY 173

FORMAT B

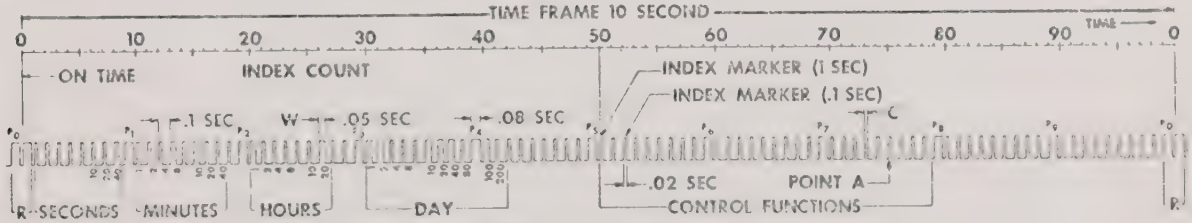
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A = 21:18:42 + .7 + .05 = 21 HRS. 18 MIN. 42.75 SEC. ON DAY 173

FORMAT E

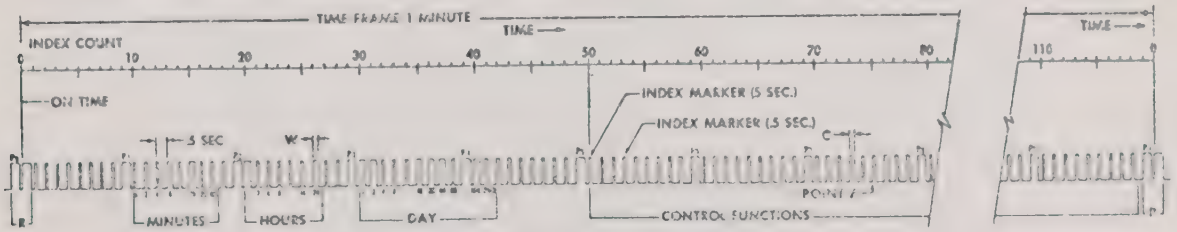
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A = 21:18:40 + .7 + .5 = 21 HR 18 MIN. 47.5 SEC. ON DAY 173

FORMAT C

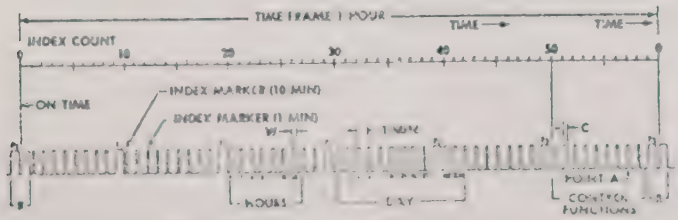
2-PPS, 23-BIT BCD TIME-OF-YEAR CODE



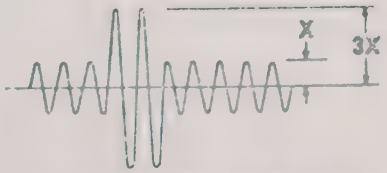
TIME AT POINT A = 21:18 + 37.5 SEC. = 21 HRS. 18 MIN. 37.5 SEC. ON DAY 173

FORMAT D

1-PPM, 16-BIT BCD TIME-OF-YEAR CODE

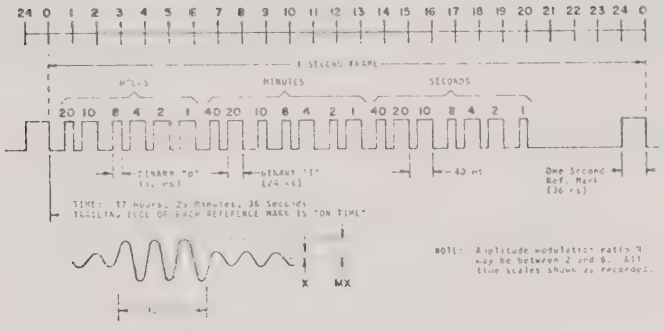


TIME AT POINT A = 21 HR. + 37 MIN. ON DAY 173



TYPICAL MODULATED SIGNAL

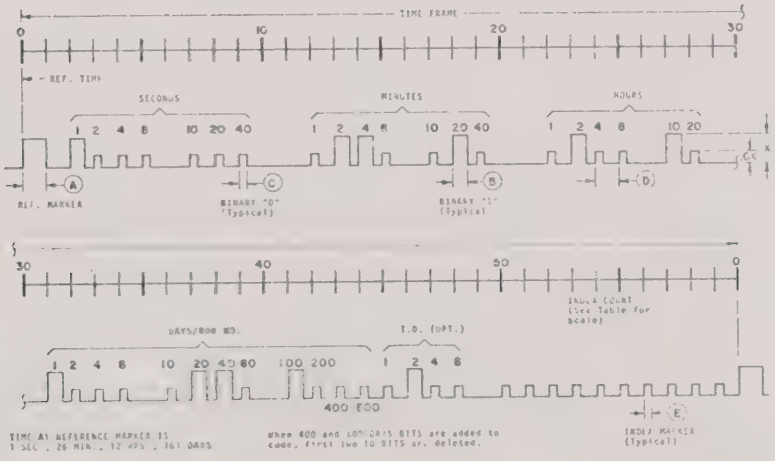
XR 3 TIME CODE FORMAT

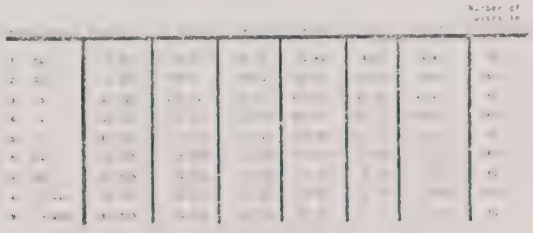

24 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 0
1 SECOND FRAME
HOURS
MINUTES
SECONDS
20 10 8 4 2 1 40 20 10 8 4 2 1 40 20 10 8 4 2 1
BINARY "0"
BINARY "1"
40 ms
One Second Ref. Mark (30 ms)
TIME: 17 Hours, 23 Minutes, 36 Seconds
TRAILING EDGE OF EACH REFERENCE MARK IS "ON TIME"
X
MX
NOTE: Amplitude modulation ratio may be between 2 and 6. All time scales shown as recorded.

TYPICAL MODULATED CODE ELEMENT "ZERO" (250 Hz Carrier)

For 1 kHz carrier large amplitude cycles number 12, 24, and 36

SLOW CODE -- TYPE "B"



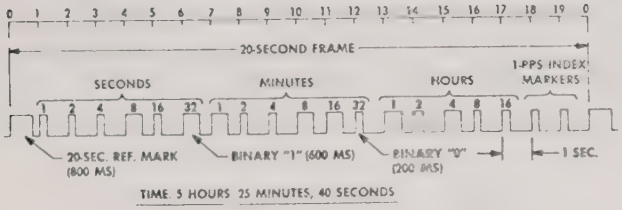


OPTIONAL CODES
and
CODE FORMATS

AMR TIME CODE FORMATS

ATLANTIC MISSILE RANGE NO. B1

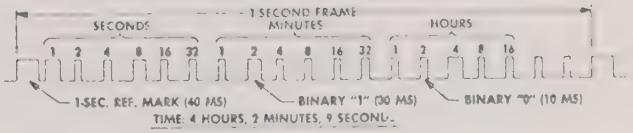
17-BIT, 1-PPS, BINARY TIME-OF-DAY CODE


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 0
20-SECOND FRAME
SECONDS
MINUTES
HOURS
1-PPS INDEX MARKERS
1 2 4 8 16 32
1 2 4 8 16 32
1 2 4 8 16
20-SEC. REF. MARK (800 MS)
BINARY "1" (600 MS)
BINARY "0" (200 MS)
1 SEC.

TIME: 5 HOURS 25 MINUTES, 40 SECONDS

ATLANTIC MISSILE RANGE NO. C1

17-BIT, 20-PPS, BINARY TIME-OF-DAY CODE



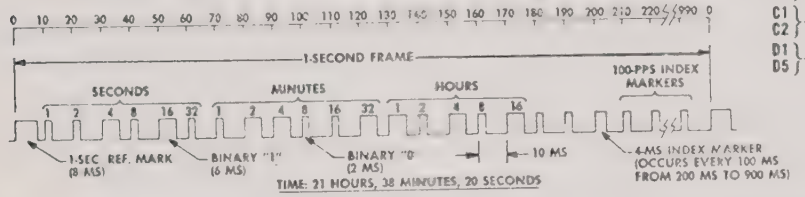
TIME: 4 HOURS, 2 MINUTES, 9 SECONDS

AMR SIGNAL DESIGNATIONS

AMR NO.	17-BIT, 24-HOUR BINARY CODE
B1	1 PPS (pulse width)
B2	1 PPS (modulated)
C1	20 PPS (pulse width)
C2	20 PPS (modulated)
D1	100 PPS (pulse width)
D5	100 PPS (modulated)

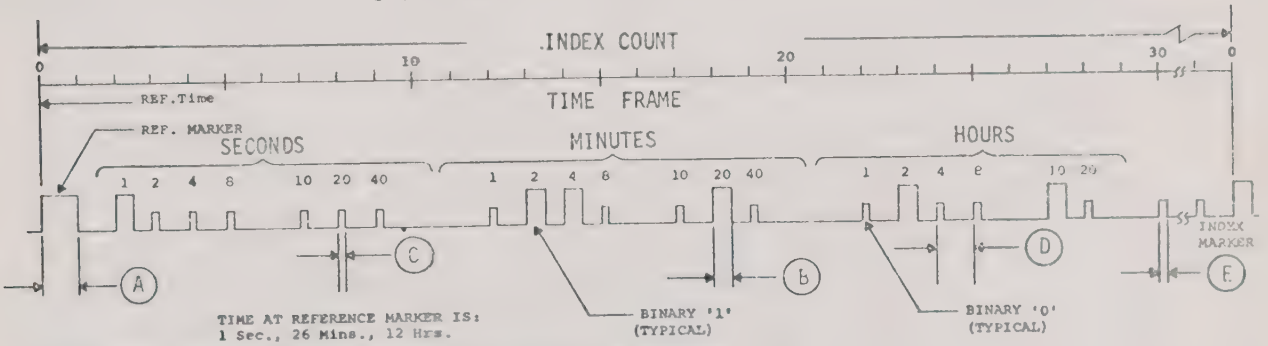
ATLANTIC MISSILE RANGE NO. D1

17-BIT, 100-PPS, BINARY TIME-OF-DAY CODE


0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 180 190 200 210 220 990 0
1-SECOND FRAME
SECONDS
MINUTES
HOURS
100-PPS INDEX MARKERS
1 2 4 8 16 32
1 2 4 8 16 32
1 2 4 8 16
1-SEC. REF. MARK (8 MS)
BINARY "1" (6 MS)
BINARY "0" (2 MS)
10 MS
4-MS INDEX MARKER (OCCURS EVERY 100 MS FROM 200 MS TO 900 MS)

TIME: 21 HOURS, 38 MINUTES, 20 SECONDS

SLOW CODE - TYPE 'A'



TIME AT REFERENCE MARKER IS:
1 Sec., 26 Mins., 12 Hrs.

	RATE	TIME FRAME	D-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec.	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs.	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs.	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	1 pps	30 Secs.	1 Sec.	1 Sec.	500 ms	200 ms	200 ms	30
5	1/2 pps	60 Secs.	2 Secs.	2 Secs.	1 Sec.	400 ms	400 ms	30
6	1/10 pps	5 Mins.	10 Secs.	10 Secs.	5 Secs.	2 Secs.	2 Secs.	30
7	1/20 pps	10 Mins.	20 Secs.	20 Secs.	10 Secs.	4 Secs.	4 Secs.	30
8	1 ppm	30 Mins.	1 Min.	1 Min.	30 Secs.	12 Secs.	12 Secs.	30
9	1/2 ppm	60 Mins.	2 Mins.	2 Mins.	1 Min.	24 Secs.	24 Secs.	30

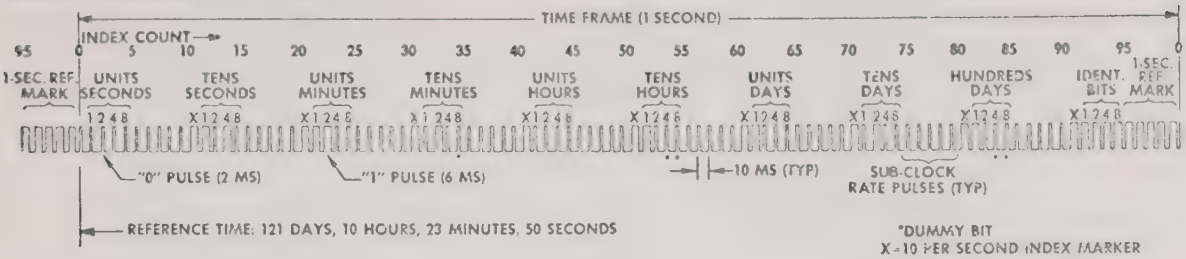
REFERENCE MARKER = 100% OF PERIOD
BINARY "1" = 50% OF PERIOD
BINARY "0" = 20% OF PERIOD
BINARY "1" AMPLITUDE = + 10V DC
BINARY "0" AMPLITUDE = + 6V DC

OPTIONAL CODES
and
CODE FORMATS

NASA TIME CODE FORMATS

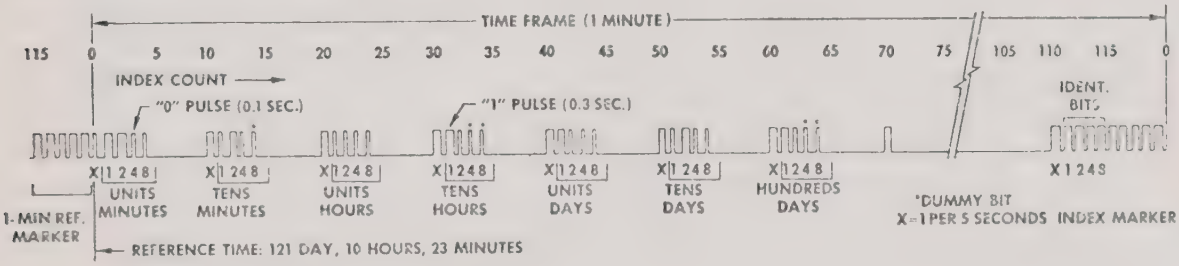
36-BIT, 100-PPS CODE (1000-CPS CARRIER)

SHOWING SUB-CLOCK RATE PULSES



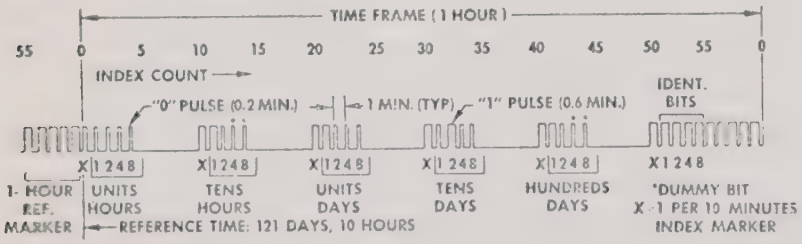
28-BIT, 2-PPS CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED

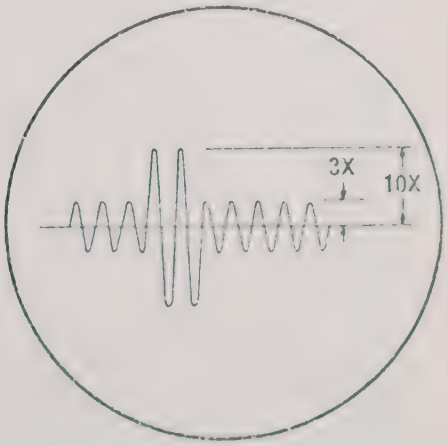

TIME FRAME (1 MINUTE)
115 0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 105 110 115 0
INDEX COUNT
"0" PULSE (0.1 SEC.)
"1" PULSE (0.3 SEC.)
IDENT. BITS
X 1 2 4 8
UNITS MINUTES
TENS MINUTES
UNITS HOURS
TENS HOURS
UNITS DAYS
TENS DAYS
HUNDREDS DAYS
1-MIN REF. MARKER
*DUMMY BIT
X=1 PER 5 SECONDS INDEX MARKER
REFERENCE TIME: 121 DAY, 10 HOURS, 23 MINUTES

20-BIT, 1-PPM CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED

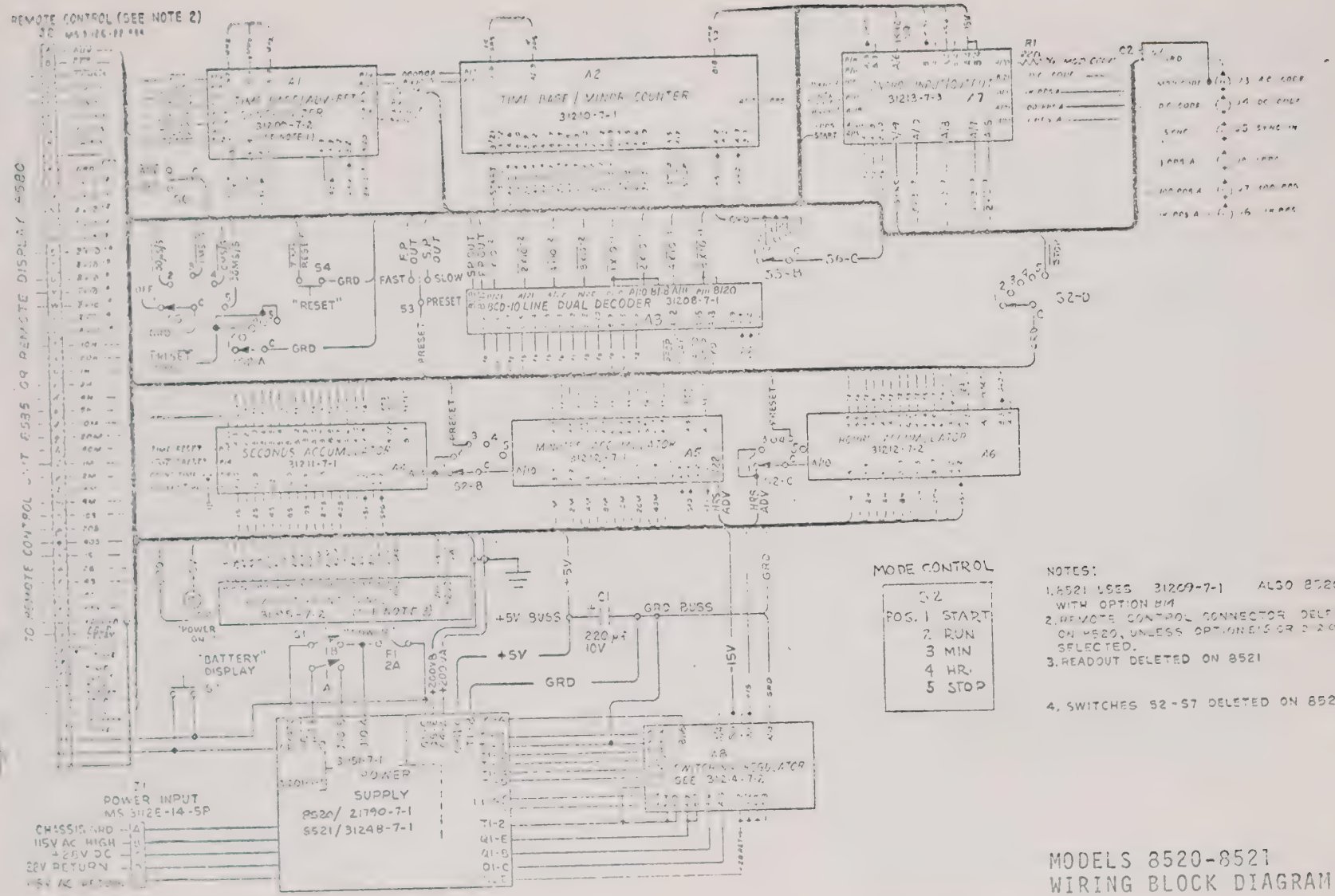


Insertion of sub-clock rate pulses is controlled for each format by individual control switches.



TYPICAL MODULATED SIGNAL

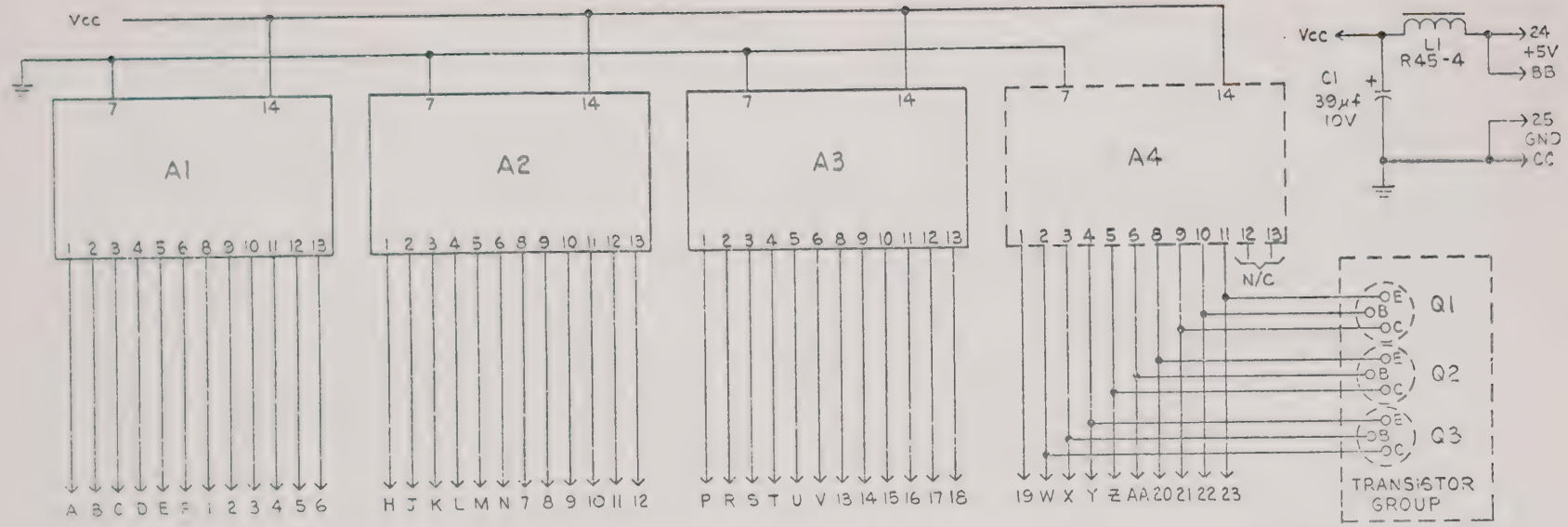
OPTIONAL CODES
and
CODE FORMATS



NOTES:

1. 8521 USES 31209-7-1 ALSO 8520 WITH OPTION #14
2. REMOTE CONTROL CONNECTOR DELETED ON 8520, UNLESS OPTIONS OR [illegible] SELECTED.
3. READOUT DELETED ON 8521
4. SWITCHES S2 - S7 DELETED ON 8521

MODELS 8520-8521
WIRING BLOCK DIAGRAM
21792-7-1



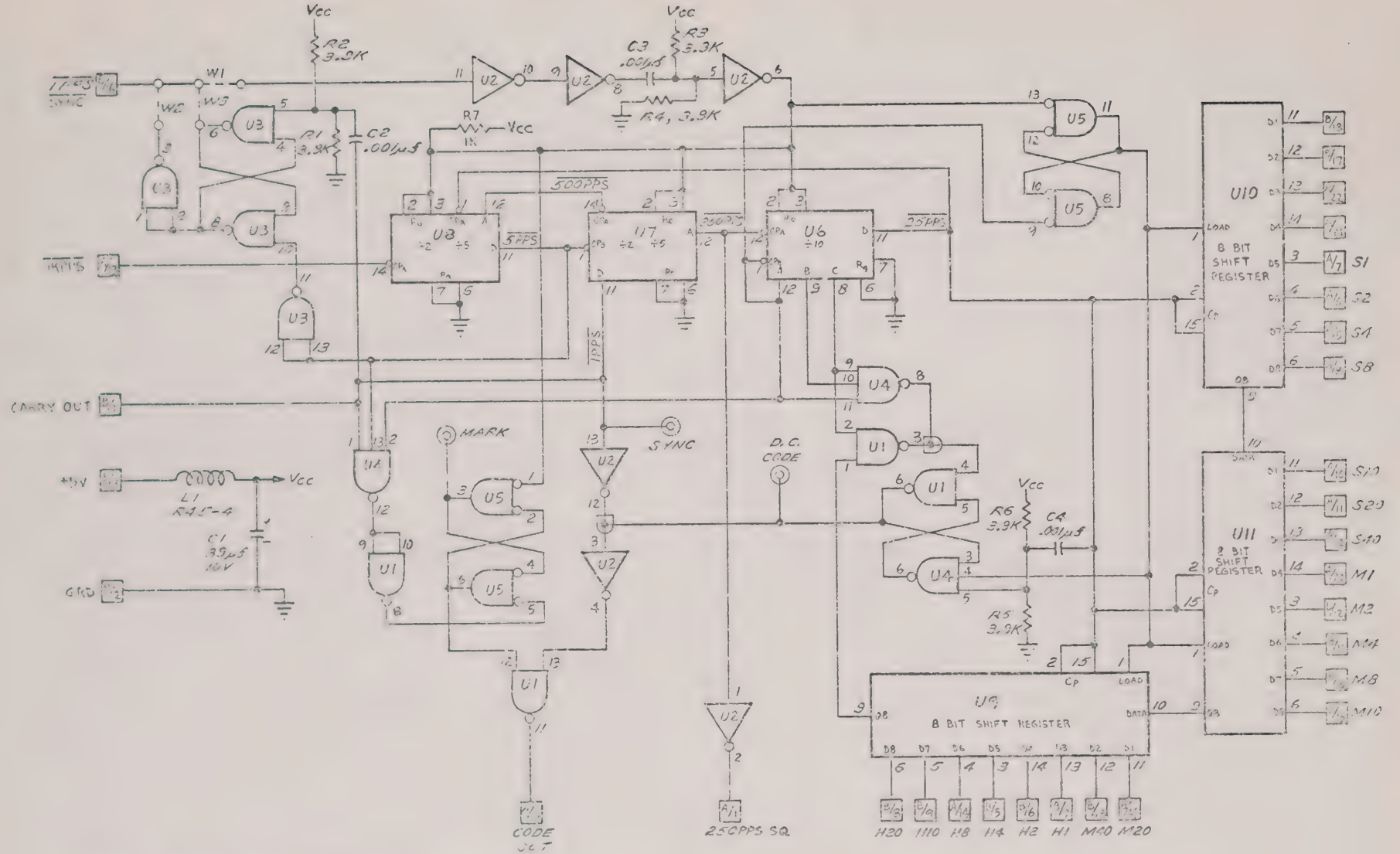
ASSY	COMPONENT COMPLEMENT						
	A1	A2	A3	A4	Q1	Q2	Q3
G45	C2155A	MC856P	MC846P	—	—	—	2N4124
G46	SN[illegible]N	SN[illegible]N	SN[illegible]N	—	2N3222	15-640	2N[illegible]
G47	MC[illegible]P	MC[illegible]P	[illegible]N5246	MC836P	—	—	—

ASSY	COMPONENT COMPLEMENT						
	A1	A2	A3	A4	Q1	Q2	Q3
G71							
G72							
G73							
G74							

UNIVERSAL LOGIC
21523-7-45 thru 70

ERRATA
DRAWINGS

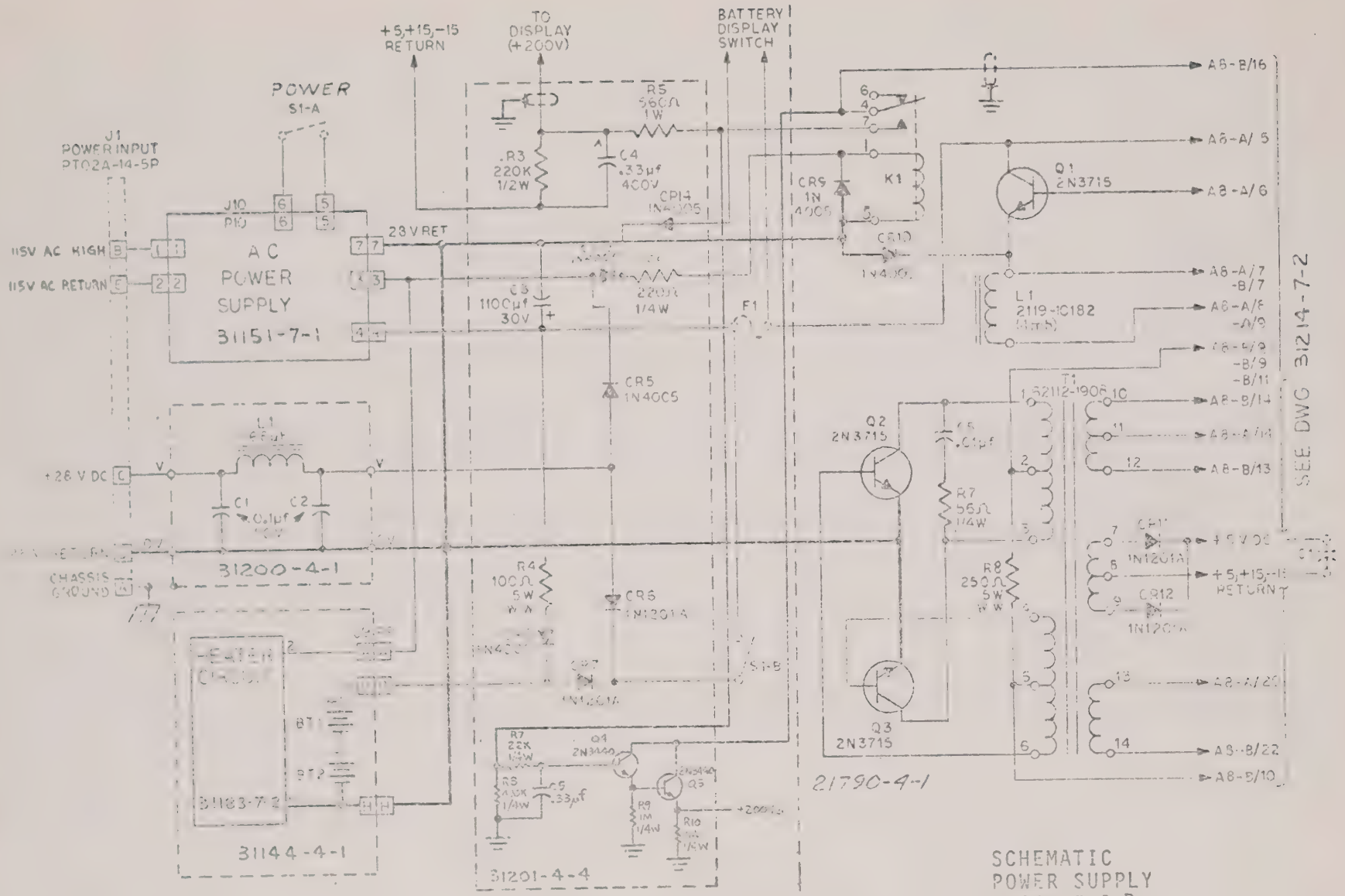
Dwg. #41046-7-1	2 of 14
Dwg. #31248-7-1	3 of 14
Dwg. #31892-7-1	4 of 14
Dwg. #41061-7-1	5 of 14
Dwg. #31033-7-1	6 of 14
Dwg. #31154-7-1	7 of 14
Dwg. #21219-4-1	8 of 14
Dwg. #21219-7-1	9 of 14
Dwg. #21223-4-1	10 of 14
Dwg. #21223-7-1	11 of 14
Dwg. #21228-4-1	12 of 14
Dwg. #31033-4-1	13 of 14
Dwg. #31154-4-1	14 of 14

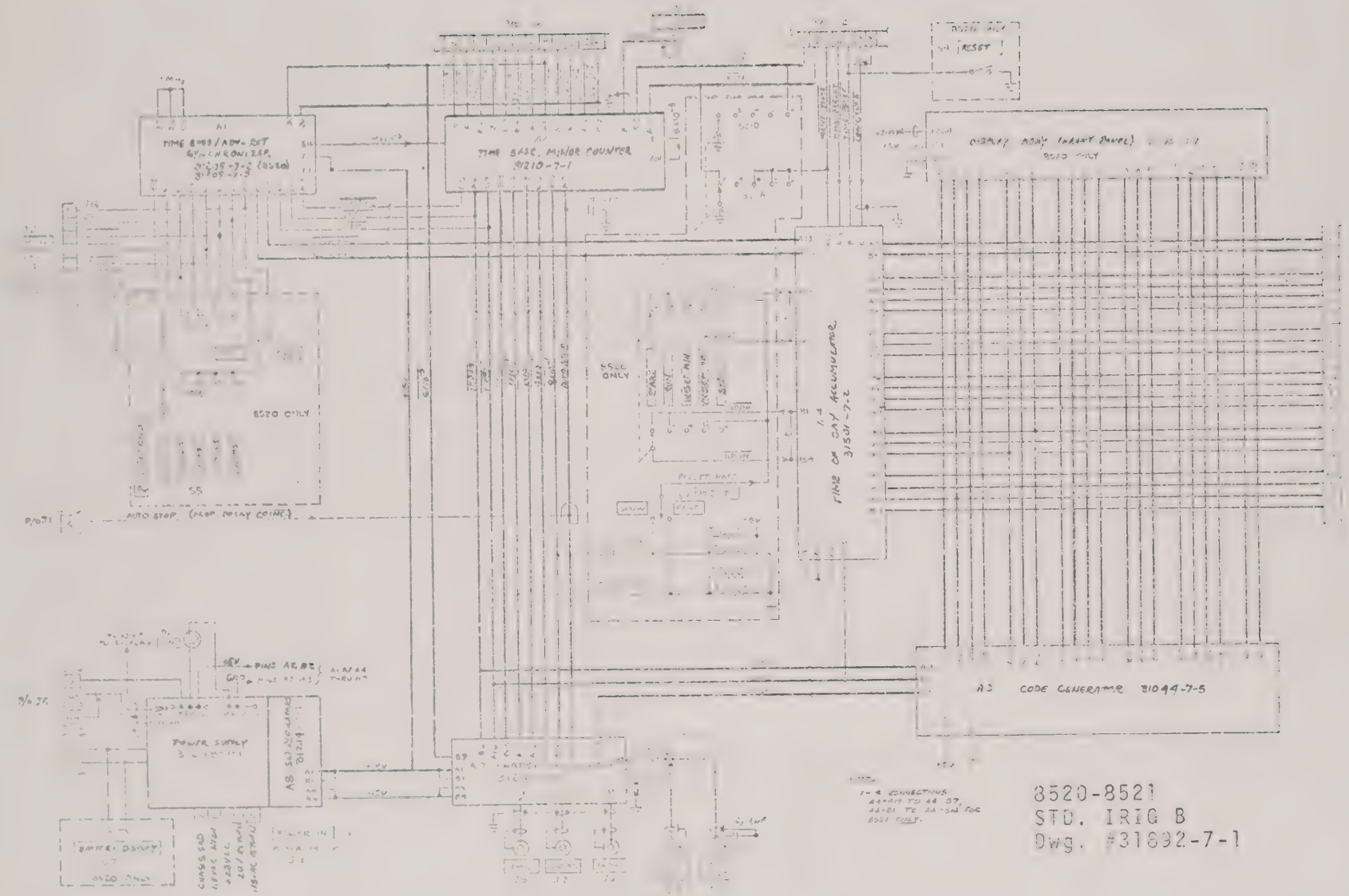


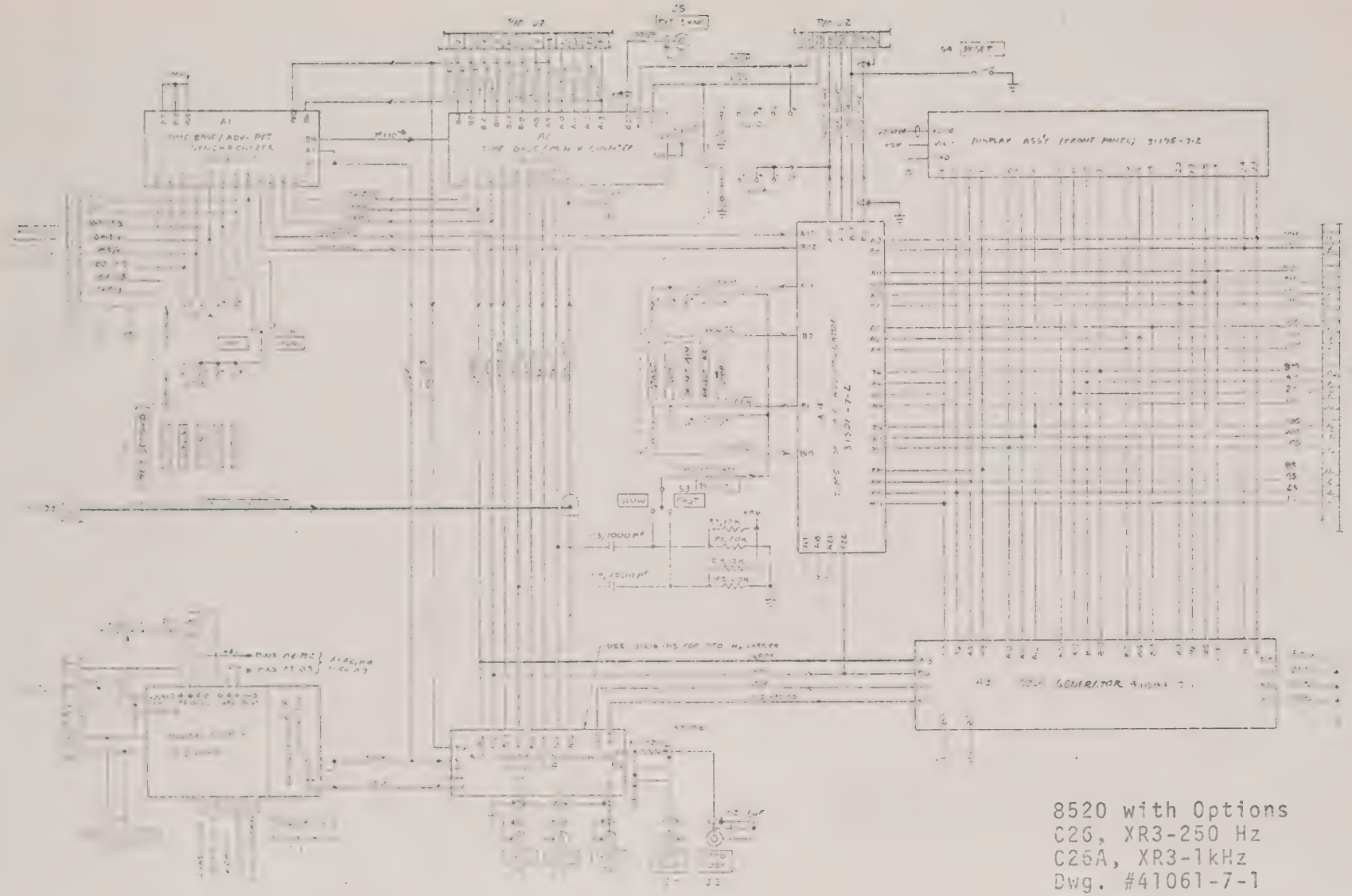
NOTES: UNLESS OTHERWISE SPECIFIED;

1. RESISTORS: ½ W, 5%, C.C.
2. ON U1 THRU U5 PIN 7 IS CONNECTED TO GRD. & PIN 14 " " " Vcc.
3. MC1810P – U5
   MC1852P – U4
   MC1813P – U2
   MC1812P – U1 & U3
4. U6 TSRU USE – SN7090N, PIN 10 IS GRD. & PIN 5 IS Vcc.
5. U9 THRU U11 – DM8200 PIN 8 IS GRD. & PIN 16 IS Vcc.

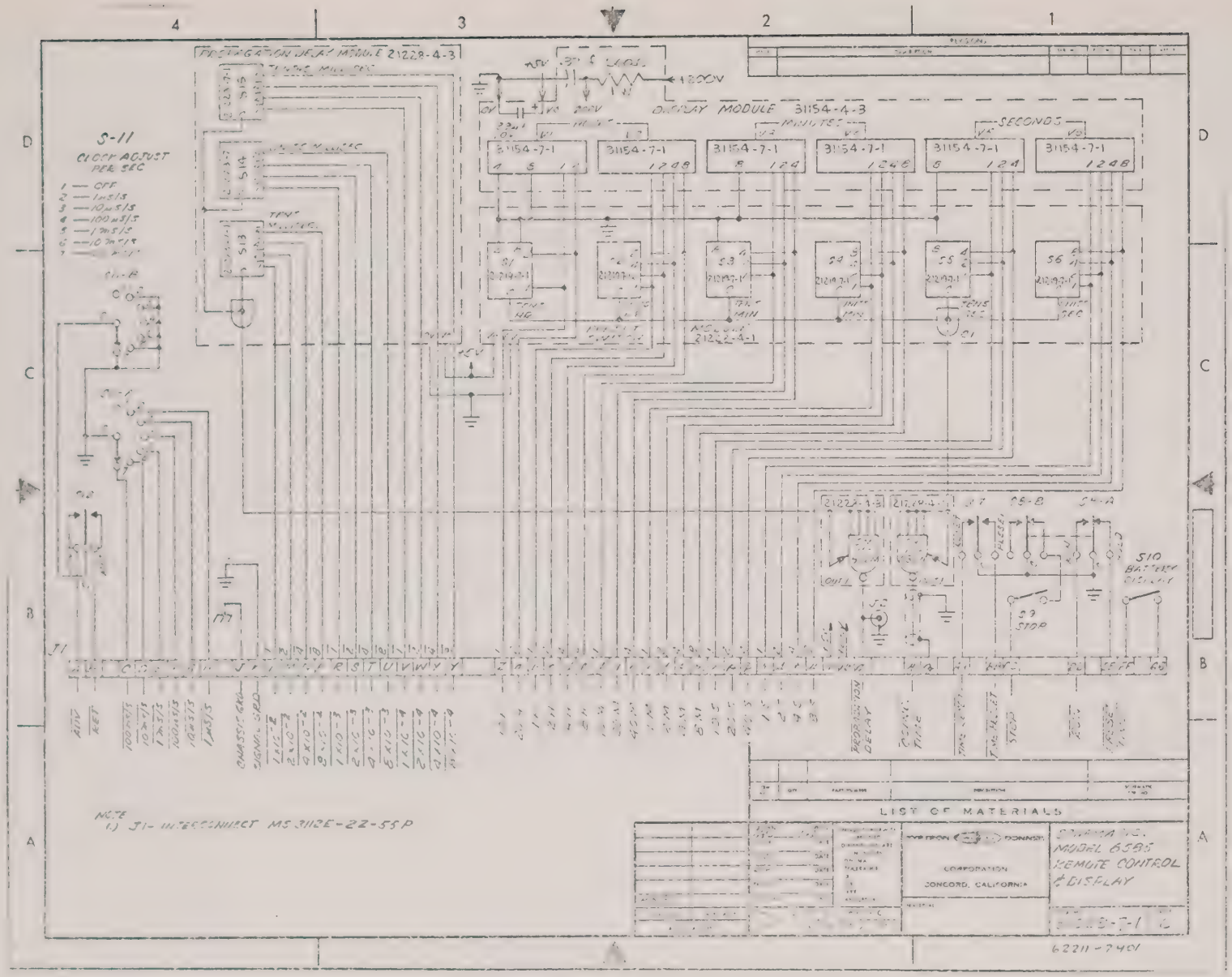
XR3 CODE GENERATOR
Dwg. #41046-7-1

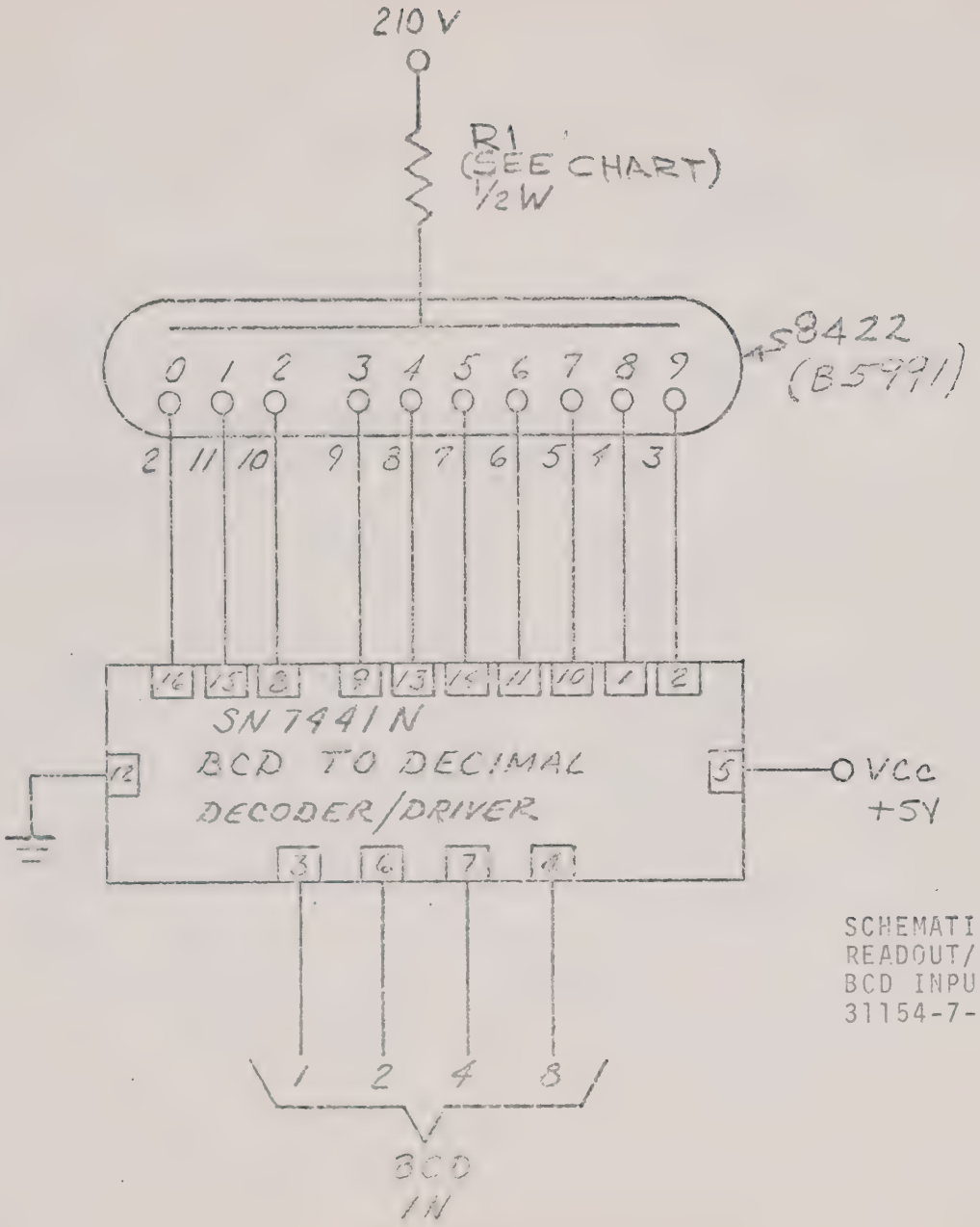

+5,+15,-15 RETURN
TO DISPLAY (+200V)
BATTERY DISPLAY SWITCH
POWER
S1-A
J1
POWER INPUT
PT02A-14-5P
J10
P10
115V AC HIGH
115V AC RETURN
AC POWER SUPPLY
31151-7-1
28 V RET
+28 V DC
CHASSIS GROUND
31200-4-1
31144-4-1
31183-7-2
31201-4-4
21790-4-1
R5 560Ω 1W
R3 220K 1/2W
C4 .33μf 400V
CR14 1N4005
CR13 1N4005
K1
Q1 2N3715
C10 1N4005
C3 1100μf 30V
R6 220Ω 1/4W
F1
CR5 1N4005
L1 2119-10182
T1 52112-1908
Q2 2N3715
Q3 2N3715
C5 .01μf
R7 56Ω 1/4W
R8 250Ω 5W WW
CR11 1N1201A
CR12 1N1201A
R4 100Ω 5W WW
CR6 1N1201A
CR7 1N1201A
R7 22K 1/2W
Q4 2N3440
R8 430K 1/4W
C9 .33μf
Q5 2N3440
R9 1M 1/4W
R10 1/4W
A8-B/16
A8-A/5
A8-A/6
A8-A/7
-B/7
A8-A/8
-A/9
-B/9
-B/11
A8-B/14
A8-A/12
A8-B/13
+5 V DC
+5,+15,-15 RETURN
A8-A/20
A8-B/22
A8-B/10
SEE DWG 31214-7-2
SCHEMATIC
POWER SUPPLY
31248-7-1 D


TIME BASE, MINOR COUNTER
8210-7-1
FINE DAY ACCUMULATOR
8150-7-2
8520 ONLY
AUTO STOP (PROG DELAY COINC)
A3 CODE GENERATOR 81049-7-5
POWER SUPPLY
8520-8521
STD. IRIG B
Dwg. #31832-7-1

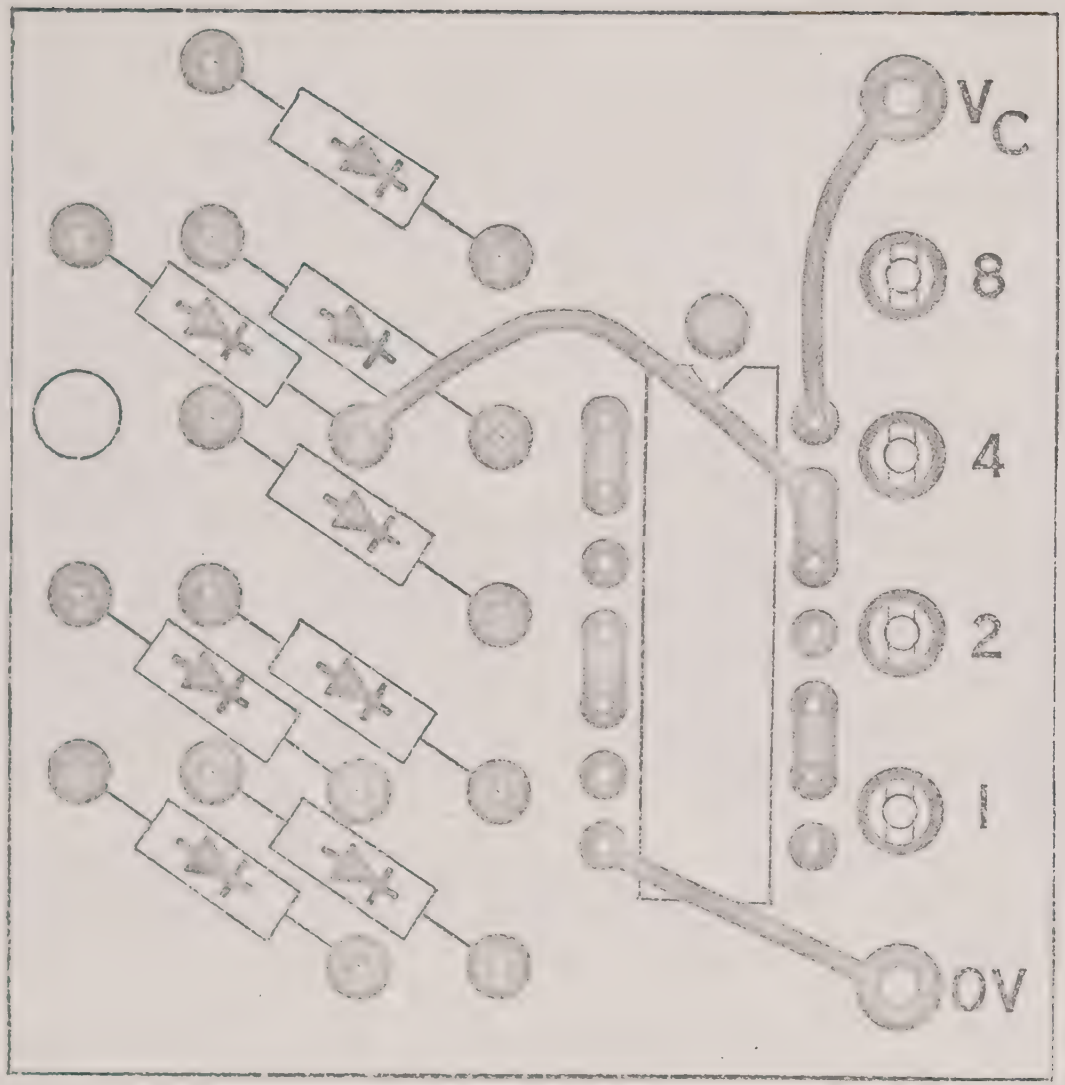


8520 with Options
C26, XR3-250 Hz
C26A, XR3-1kHz
Dwg. #41061-7-1

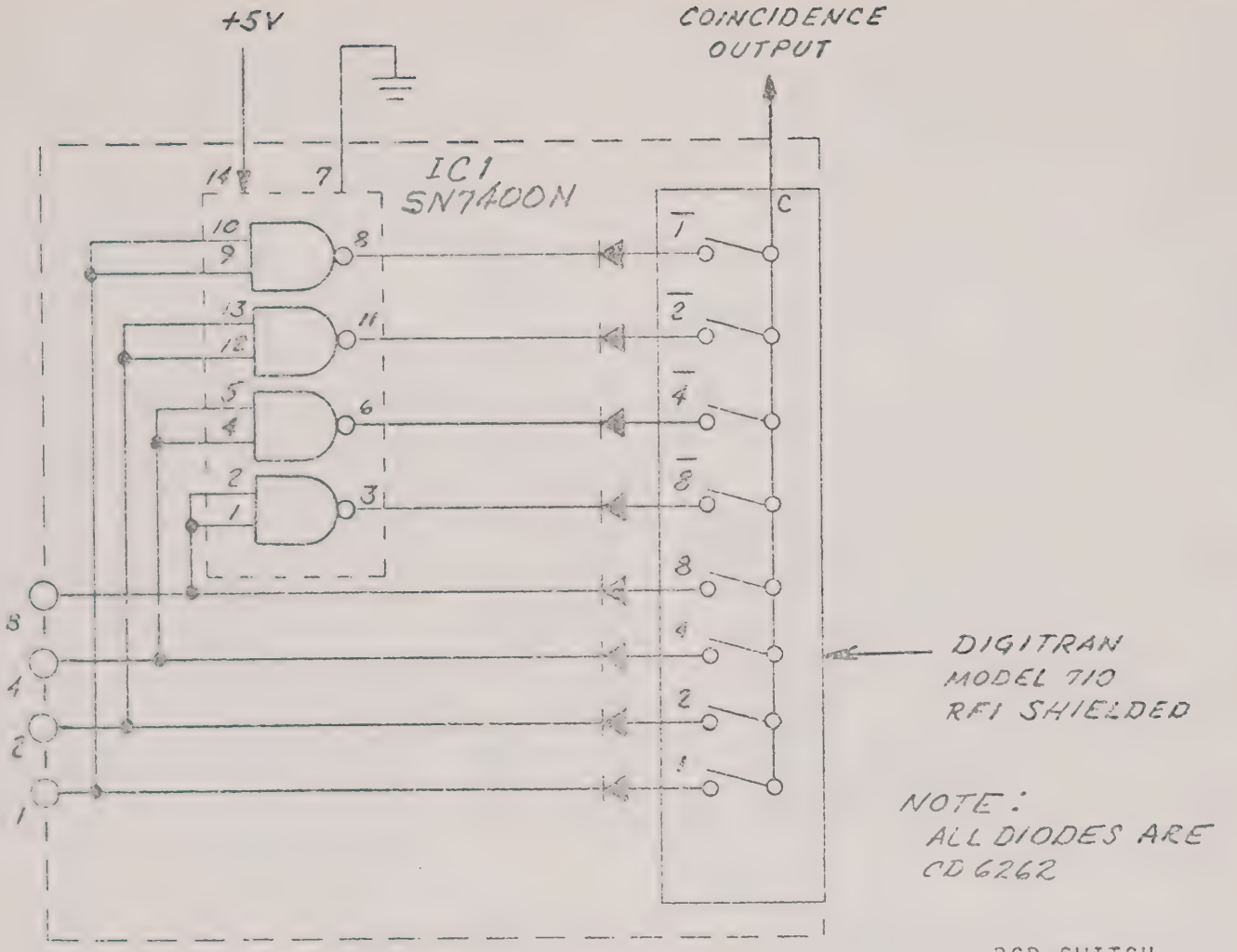

DELAY MODULE 31154-4-3
SECONDS
MINUTES
S-11
CLOCK ADJUST PER SEC
LIST OF MATERIALS
NOTE
1.) J1- INTERCONNECT MS3112E-22-55P
SONICA INC.
MODEL 6585
REMOTE CONTROL & DISPLAY
CONCORD, CALIFORNIA
62211-7401



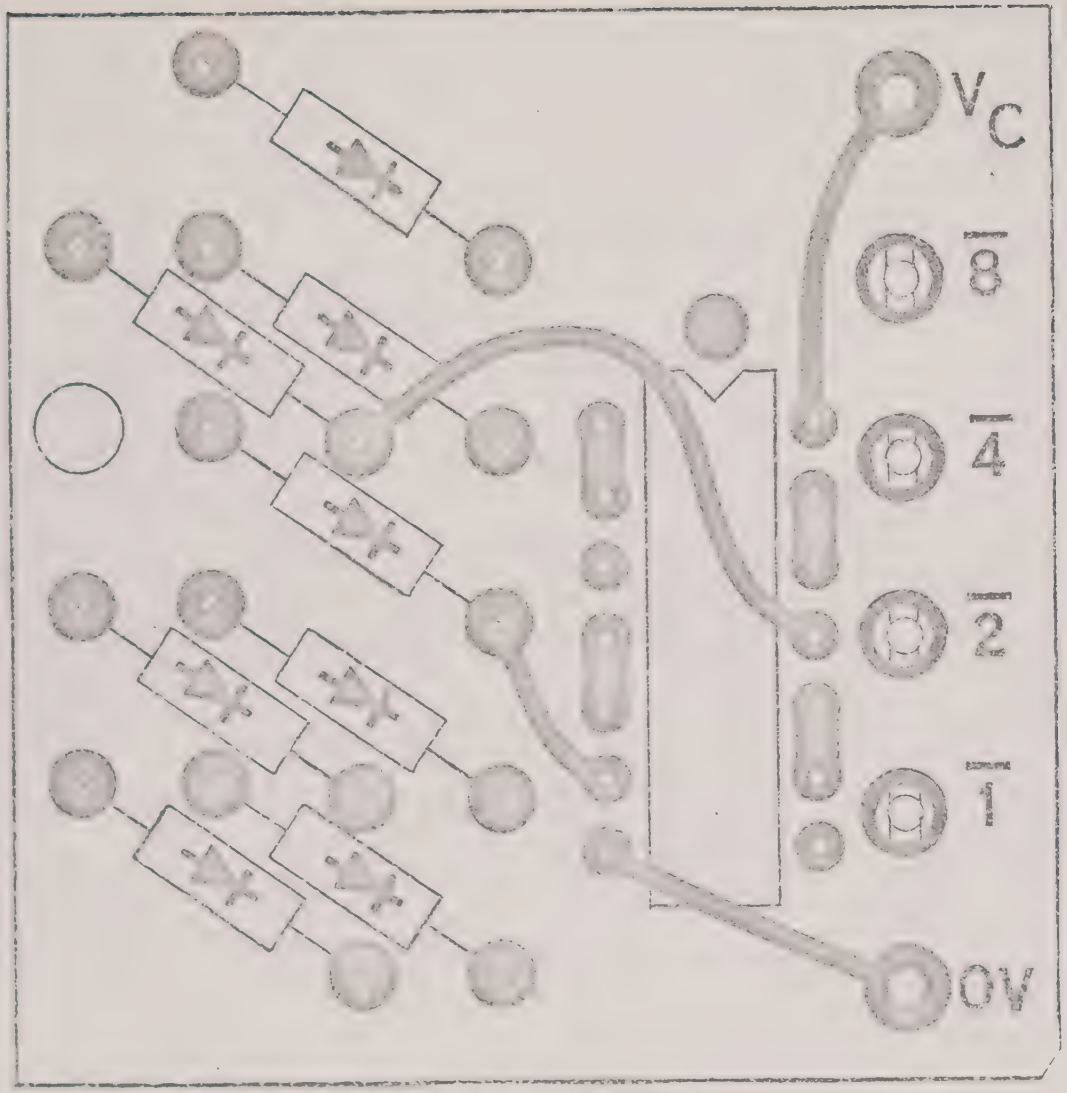
SCHEMATIC
READOUT/DECODER
BCD INPUT
31154-7-1 B



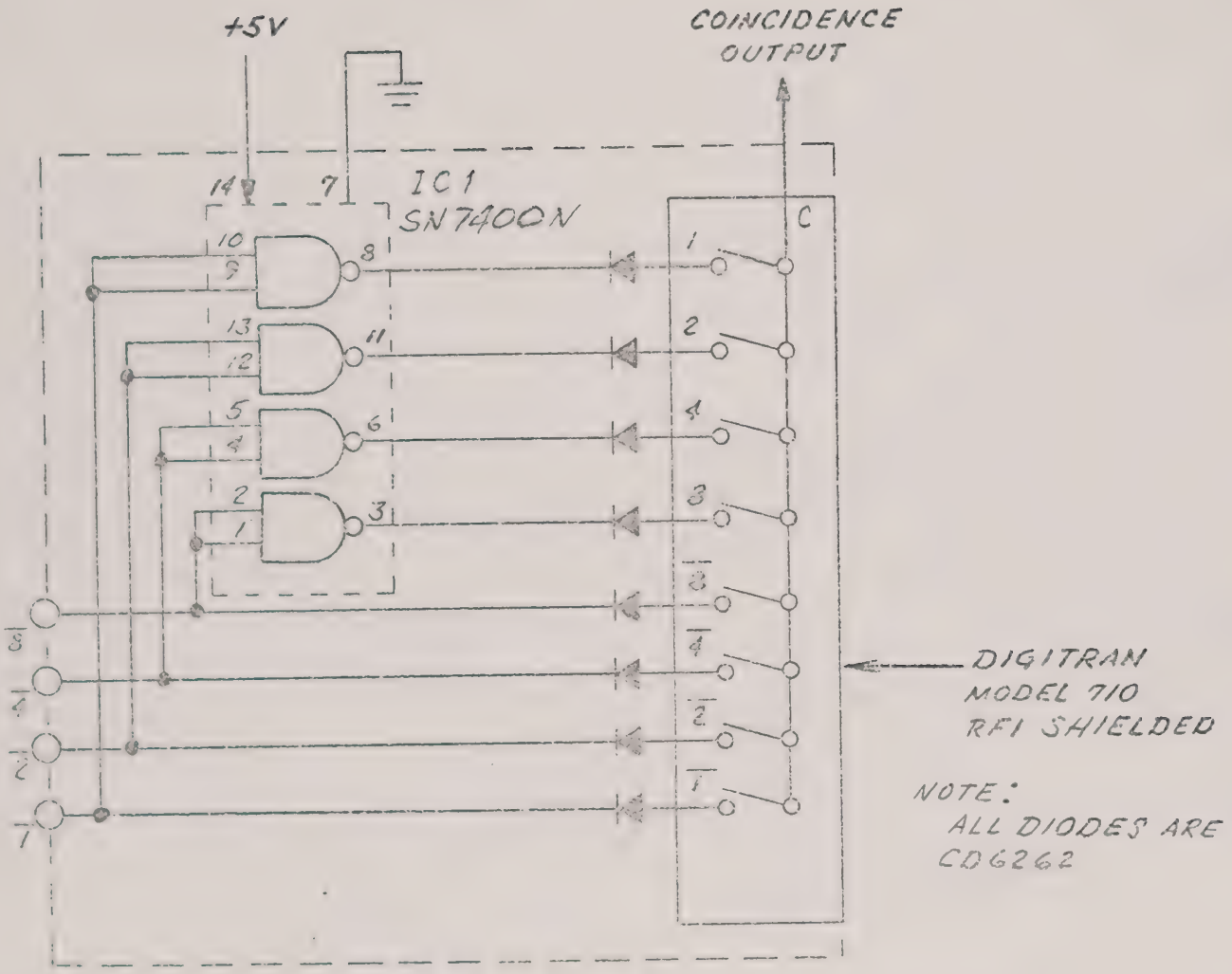
ASSEMBLY
SWITCH INVERTER
(1, 2, 4, 8)
Dwg. # 21219-4-1



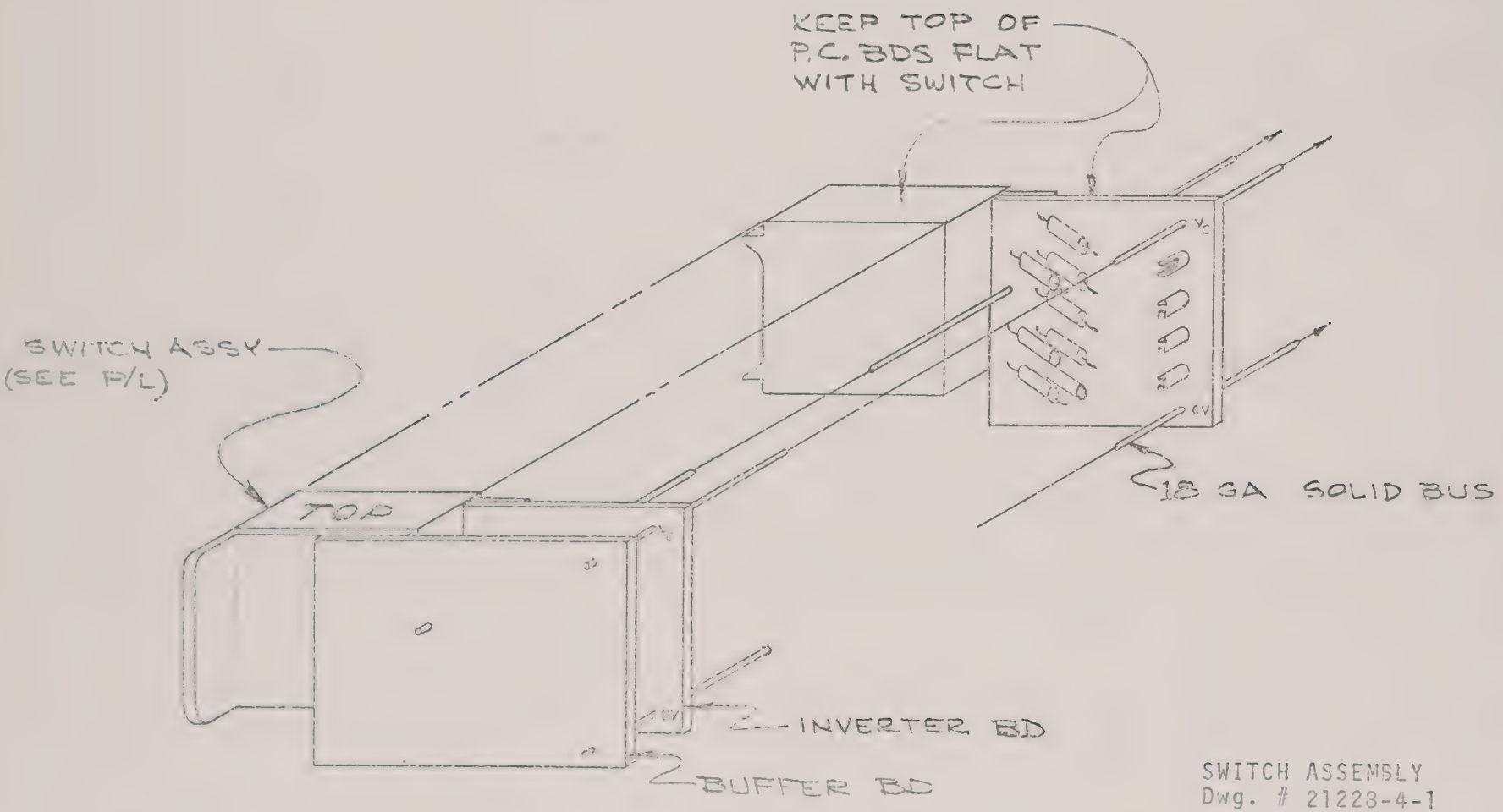
BCD SWITCH
INVERTER
(1, 2, 4, 8)
Dwg. #21219-7-1



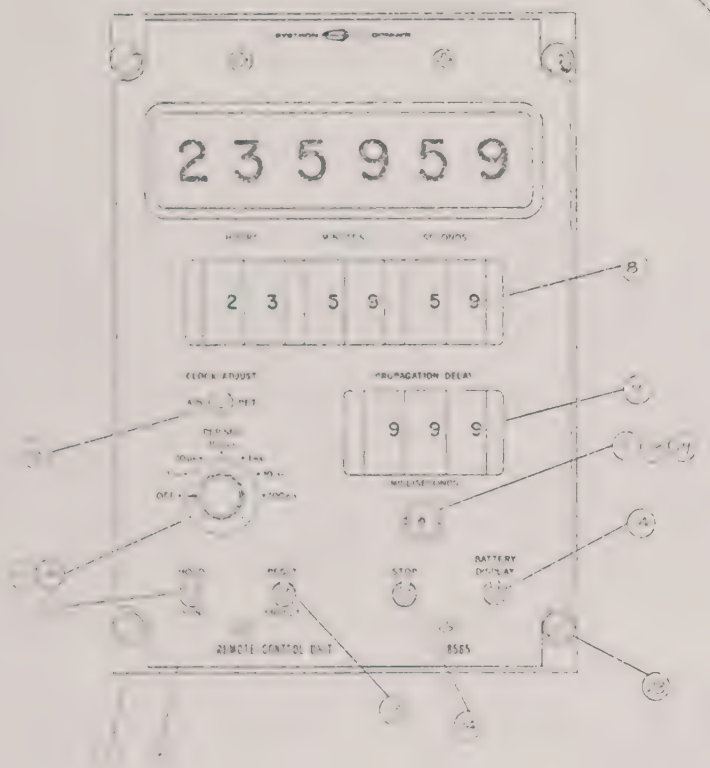
ASSEMBLY
SWITCH INVERTER
($\overline{1}$, $\overline{2}$, $\overline{4}$, $\overline{8}$)
Dwg. #21223-4-1

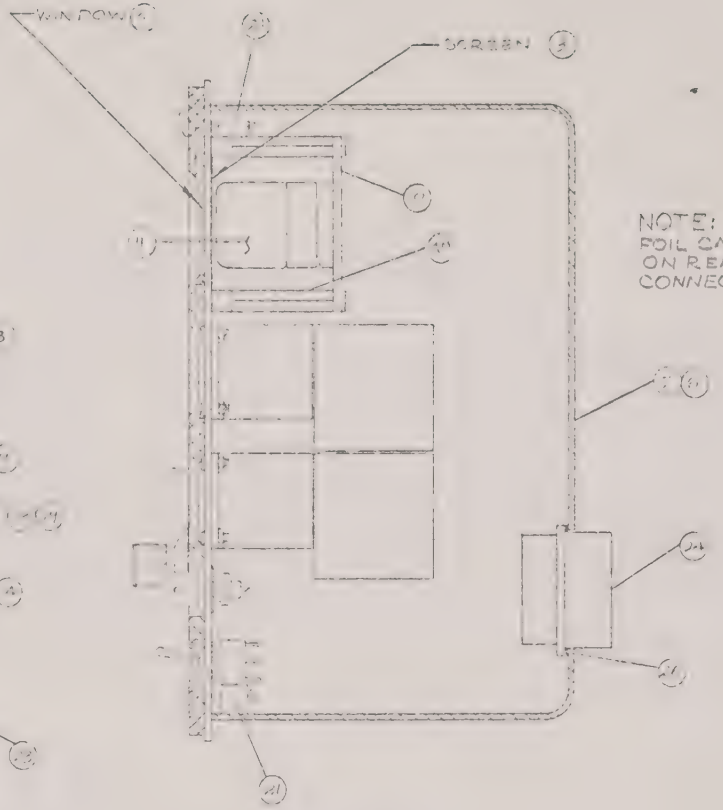


BCD SWITCH
INVERTER
($\overline{1}$, $\overline{2}$, $\overline{4}$, $\overline{8}$)
Dwg. #21223-7-1



SWITCH ASSEMBLY
Dwg. # 21228-4-1





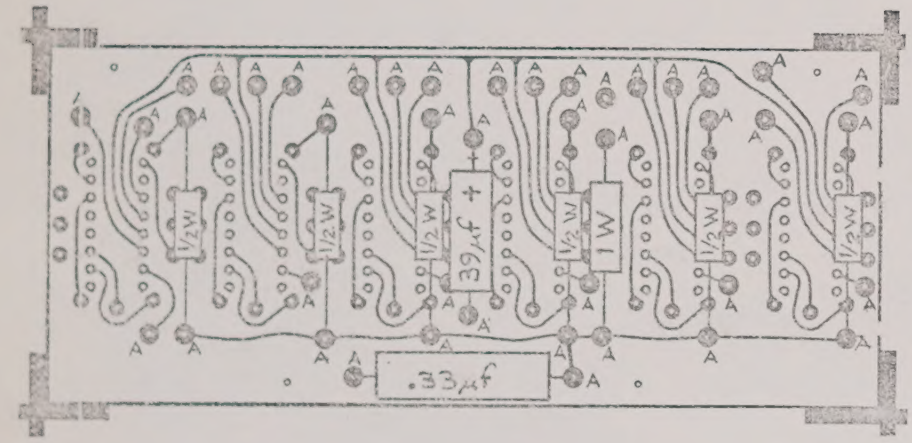
NOTE:
FOIL CAL CENTERED ON REAR 1" ABOVE CONNECTOR

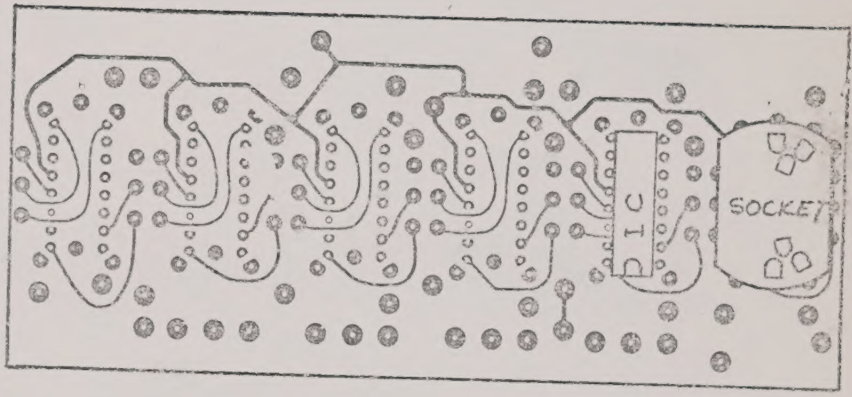
LIST OF MATERIALS

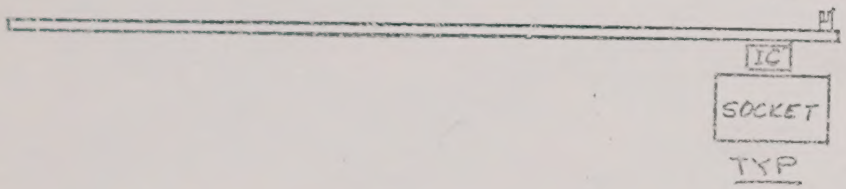
SYSTRON DONNER CORPORATION
CONCORD, CALIFORNIA

REMOTE ASSY

62211-4400







ASSEMBLY
READOUT
(0.790 CENTERS)
31154-4-1 A

MP MASTER
MA34104